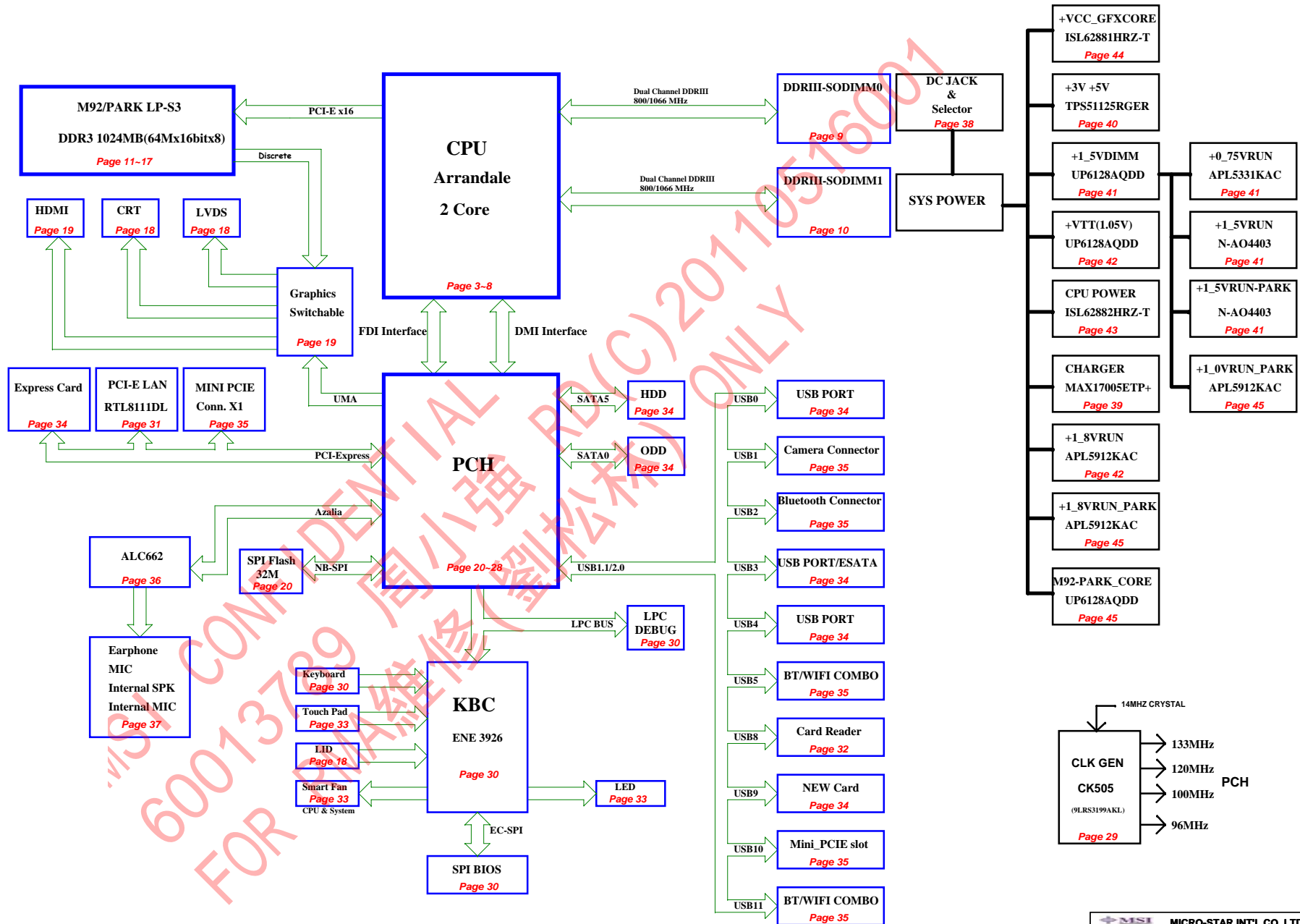


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29 : Clock Generator (9LRS3199AKL)
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

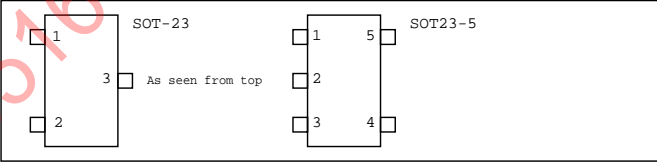
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN DDRIII core PCH DDRIII command & control pull up. CPU core rail Graphics core rail (Dual Core only)
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V-1.1V	S0	
+VCC_GFXCORE	1.1V	S0	
M92S_VDD_CORE	0.95V	S0	GPU core power GPU PCIE power GPU DDR3 power GPU PCIE power GPU I/O and DAC power
+1_8VRUN_PARK	1.8V	S0	
+1_5VRUN_PARK	1.5V	S0	
+1_0VRUN_PARK	1.0V	S0	
VDDR3	3.3V	S0	

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



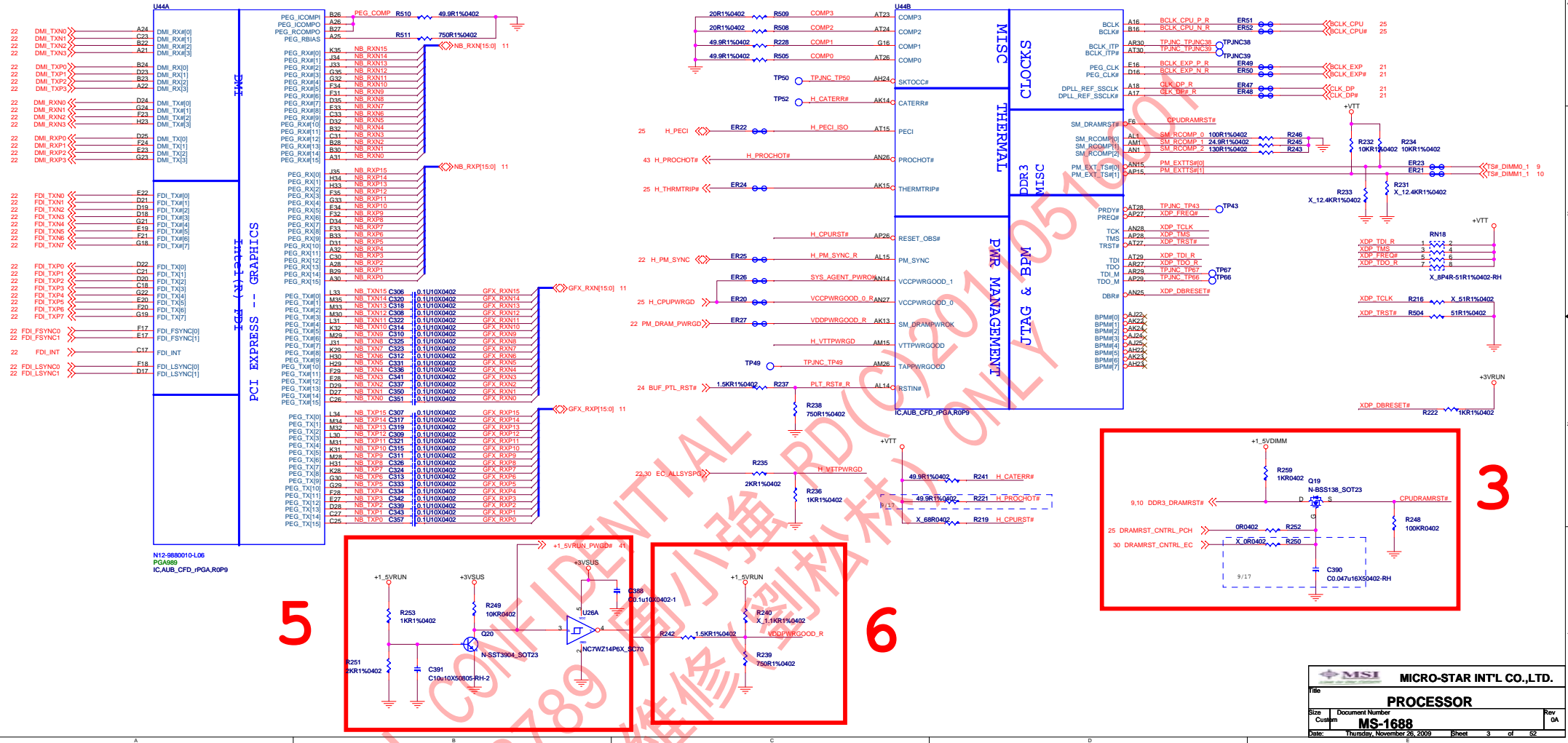
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

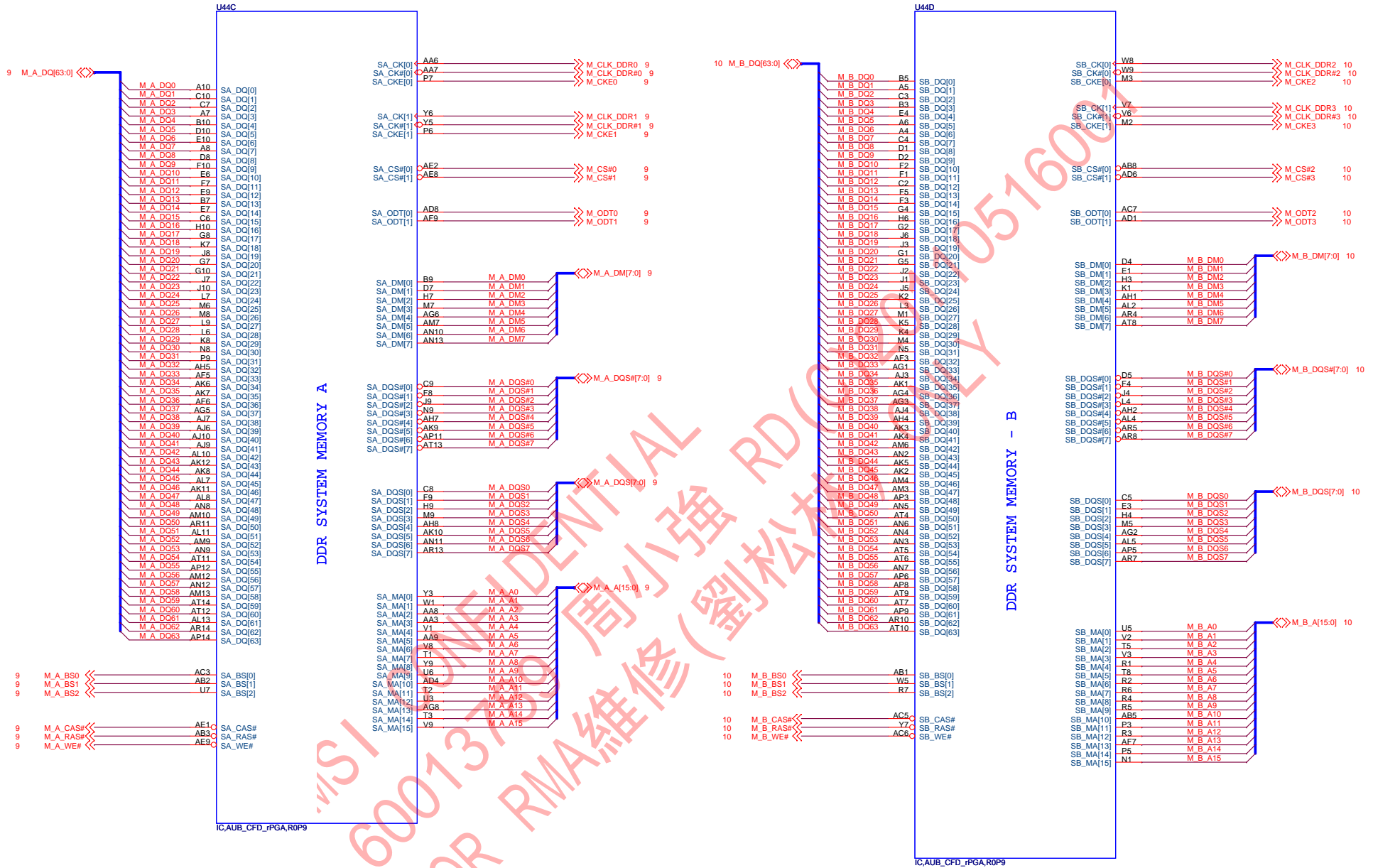
Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUIN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



ARRANDALE PROCESSOR (DDR3)



ARRANDALE PROCESSOR (POWER)

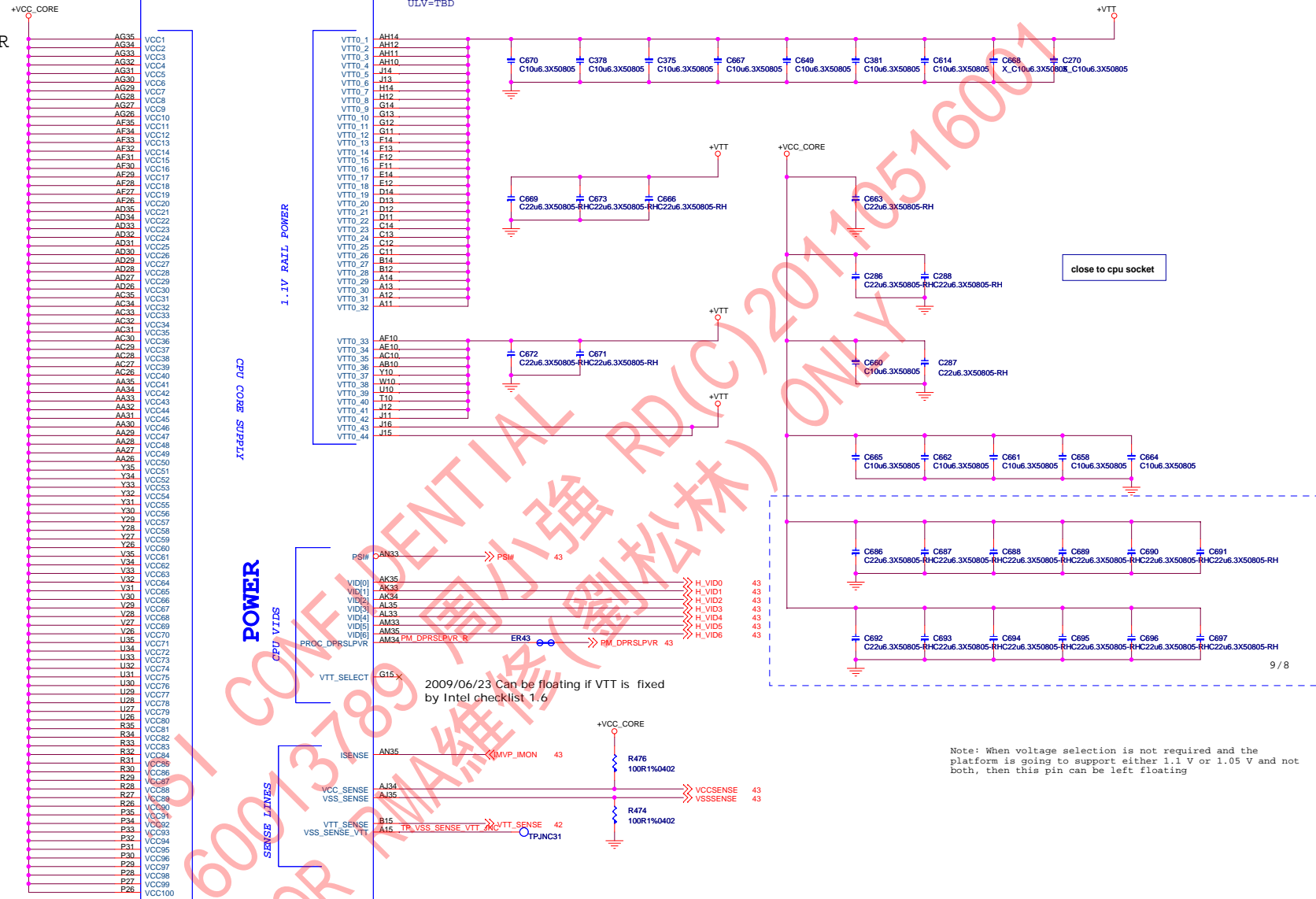
ARRANDALE:
SV=48A
LV=35A
ULV=27A

U44F

ARRANDALE:
SV=18A
LV=TBD
ULV=TBD

PROCESSOR CORE POWER

PROCESSOR CORE POWER



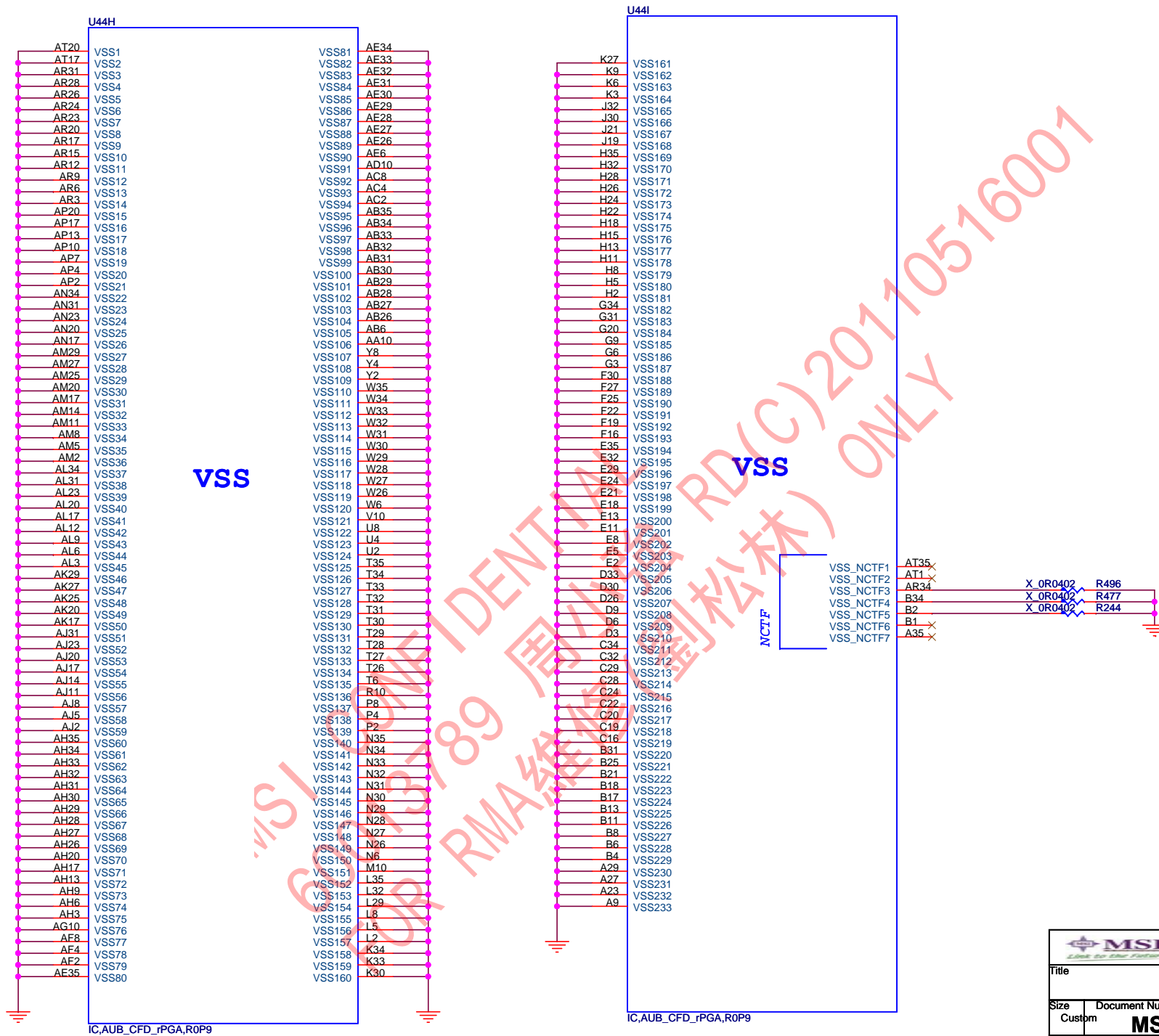
Note: When voltage selection is not required and the platform is going to support either 1.1 V or 1.05 V and not both, then this pin can be left floating

MICRO-STAR INT'L CO.,LTD.

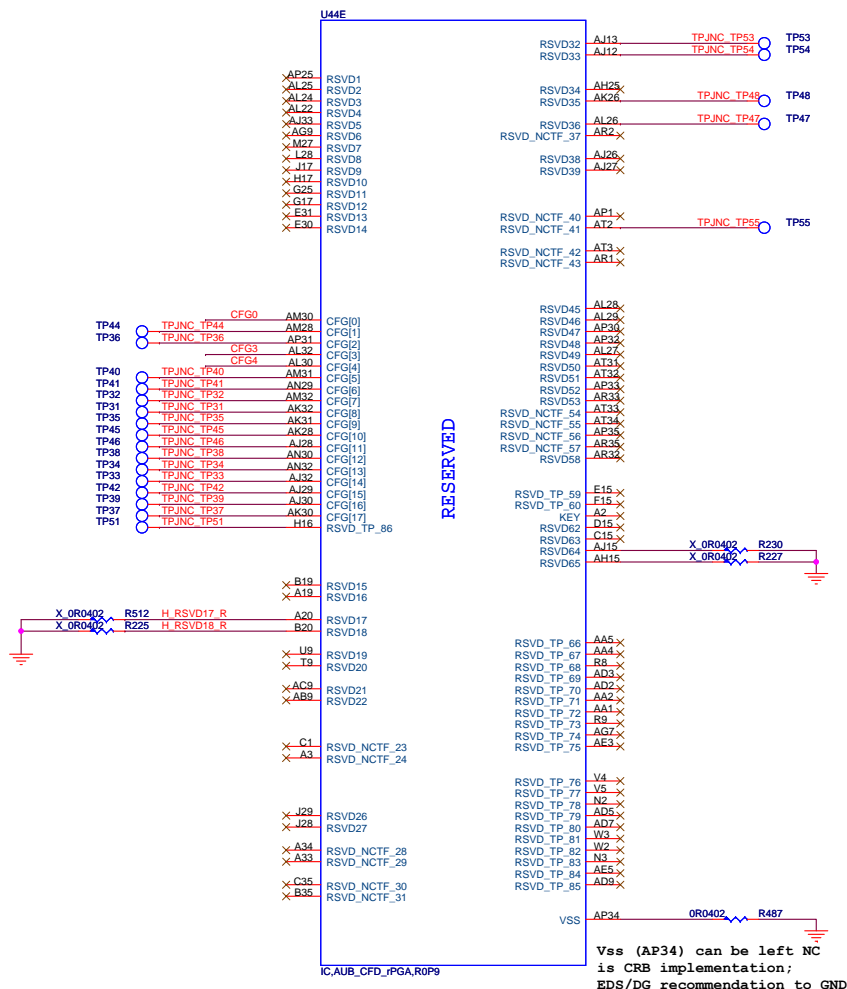
PROCESSOR POWER			
Size	Document Number	Rev	
Custom	MS-1688	0A	
Date:	Thursday, November 26, 2009	Sheet	5 of 52

[illegible]

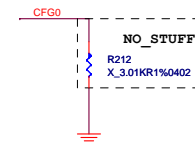
ARRANDALE PROCESSOR (GND)



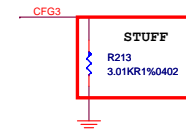
ARRANDALE PROCESSOR (RESERVED)



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

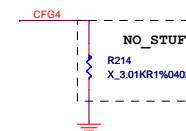


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG[3] - PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
 • 1: No lane reversal
 • 0: Reversal

CFG4 - Display Port Presence	
CFG4	1:Disabled: No Physical Display Port attached to Embedded Display Port 0:Enabled: An external Display Port device is connected to the Embedded Display Port

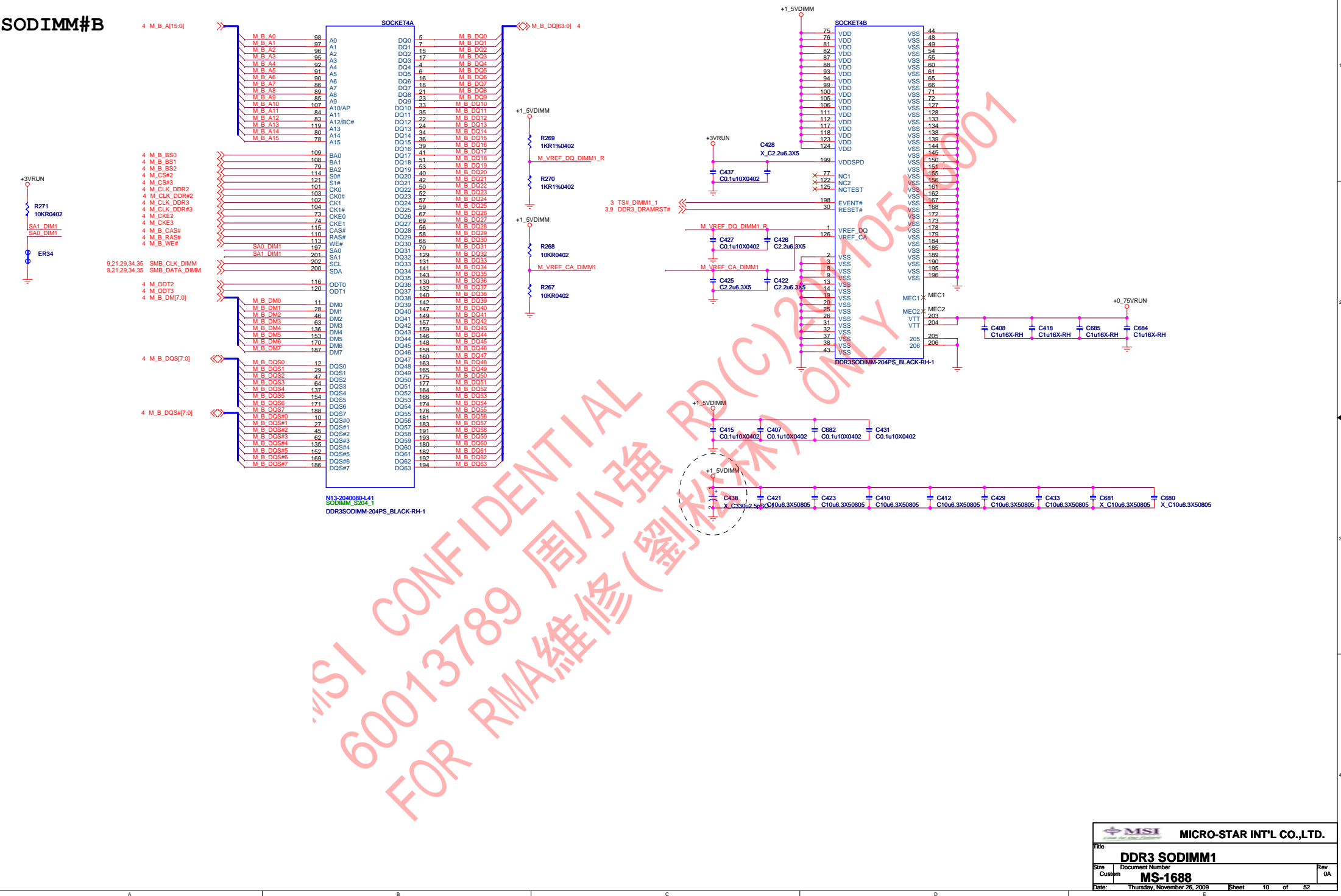


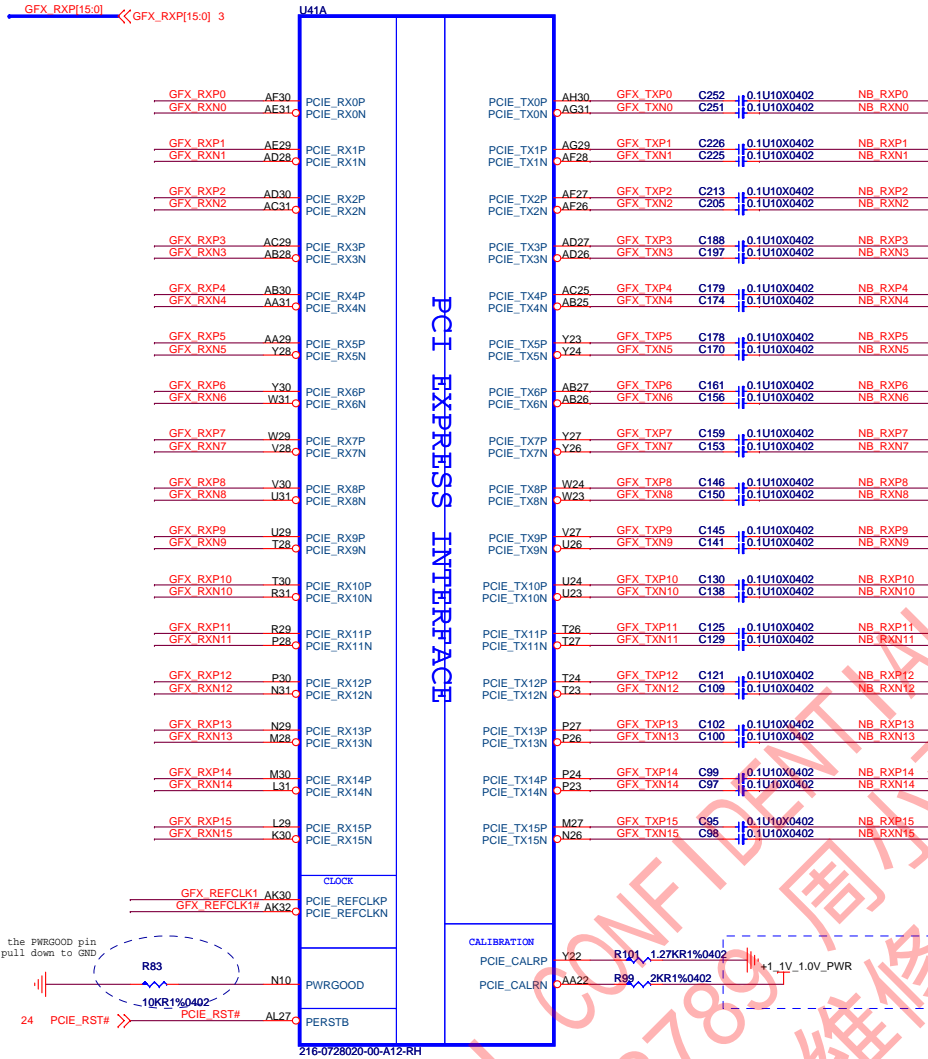
Layout Note:
Location of all CFG strap resistors needs to be close to trace to minimize stub

SODIMM#A

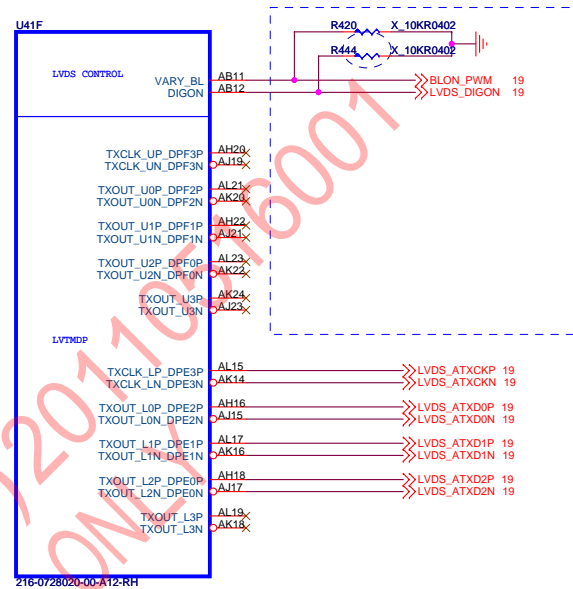


SODIMM#B

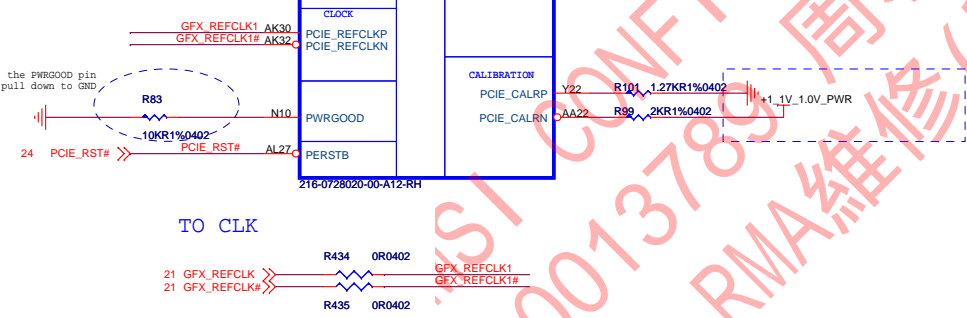




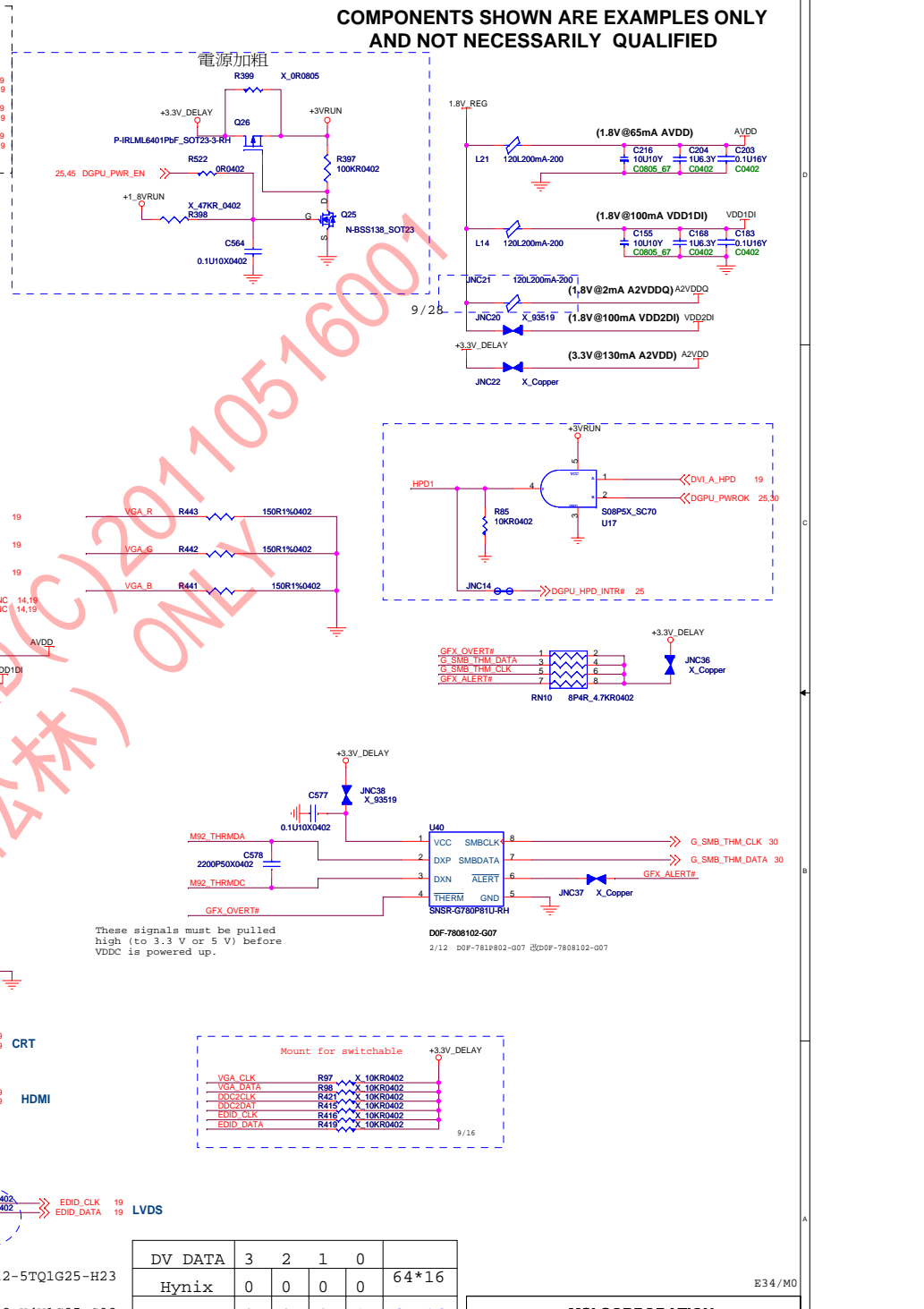
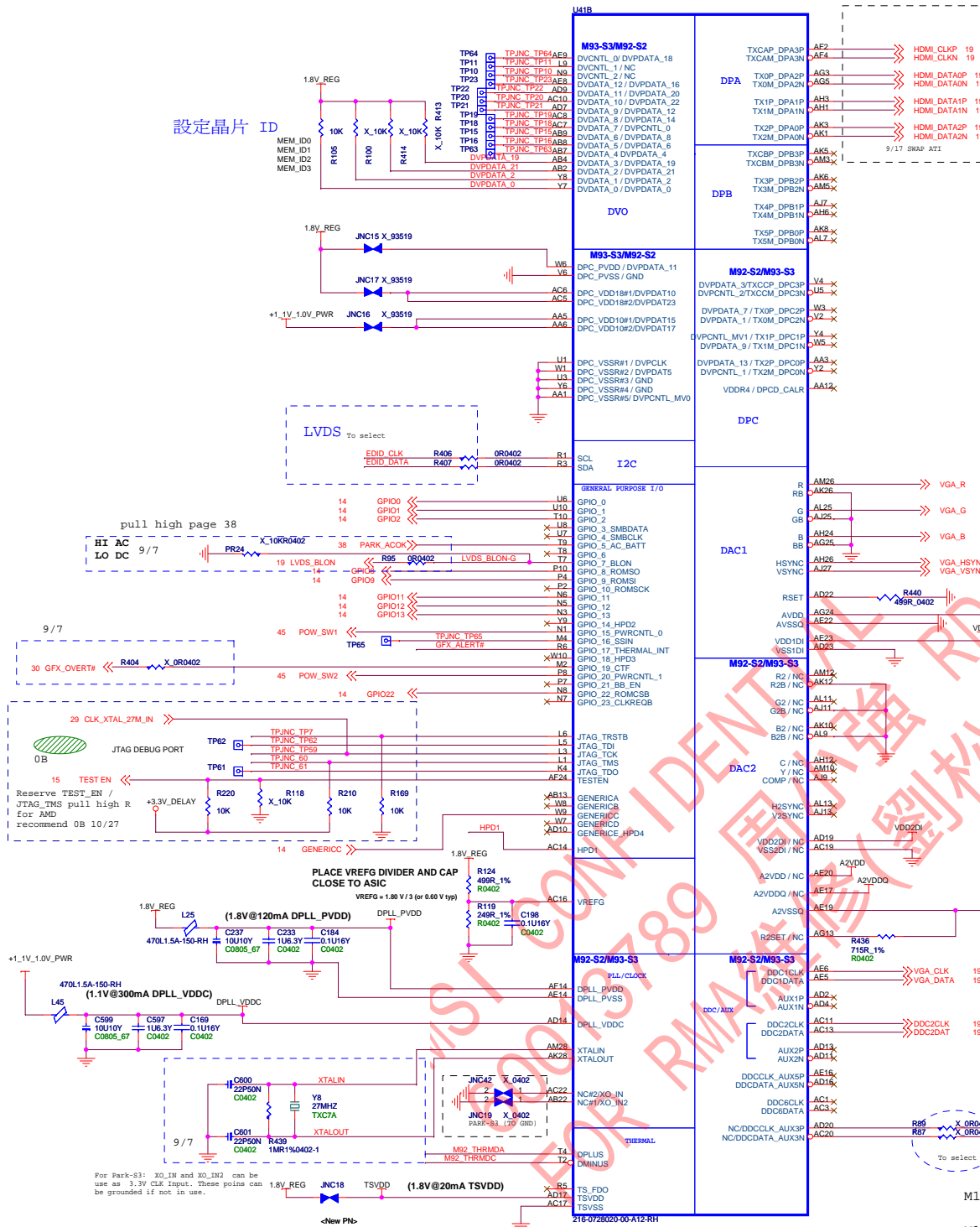
LVDS Interface



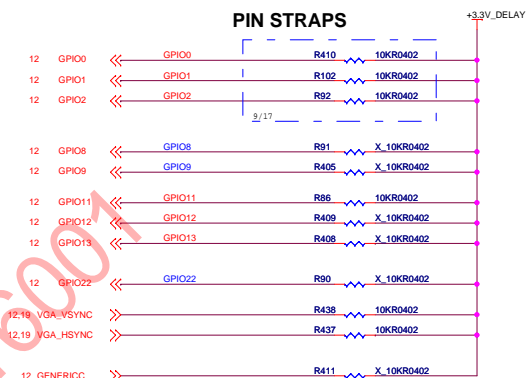
DisplayPort E Configuration



設定晶片 ID



DV DATA	3	2	1	0	
Hynix	0	0	0	0	64*16
SAMSUNG	0	0	0	1	64*16



ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYSN	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

GPIO 13, 12, 11	
Size of the primary memory apertures	CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
512 MB ^{10 MB}	001

Due to memory management constraints, the aperture size should be the same size as the frame buffer for 64 MB, 128 MB and 256 MB. For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.

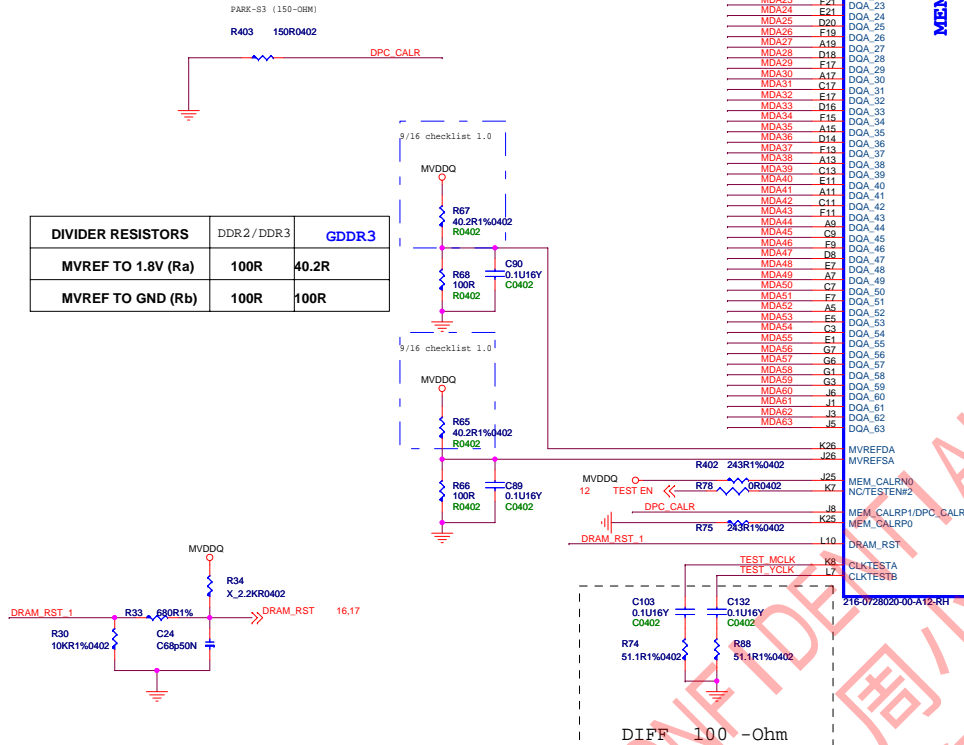
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
<p>GPIQ21_BB_EN</p>	

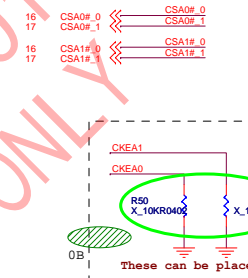
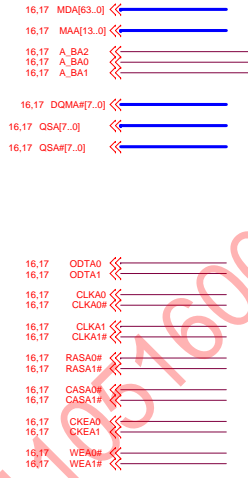
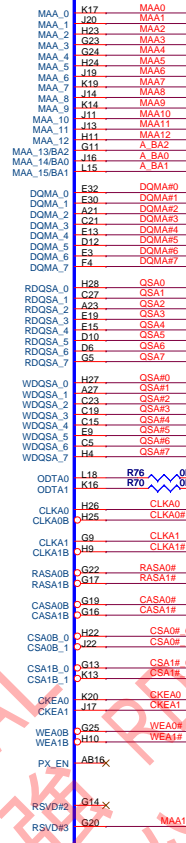
E23/M0

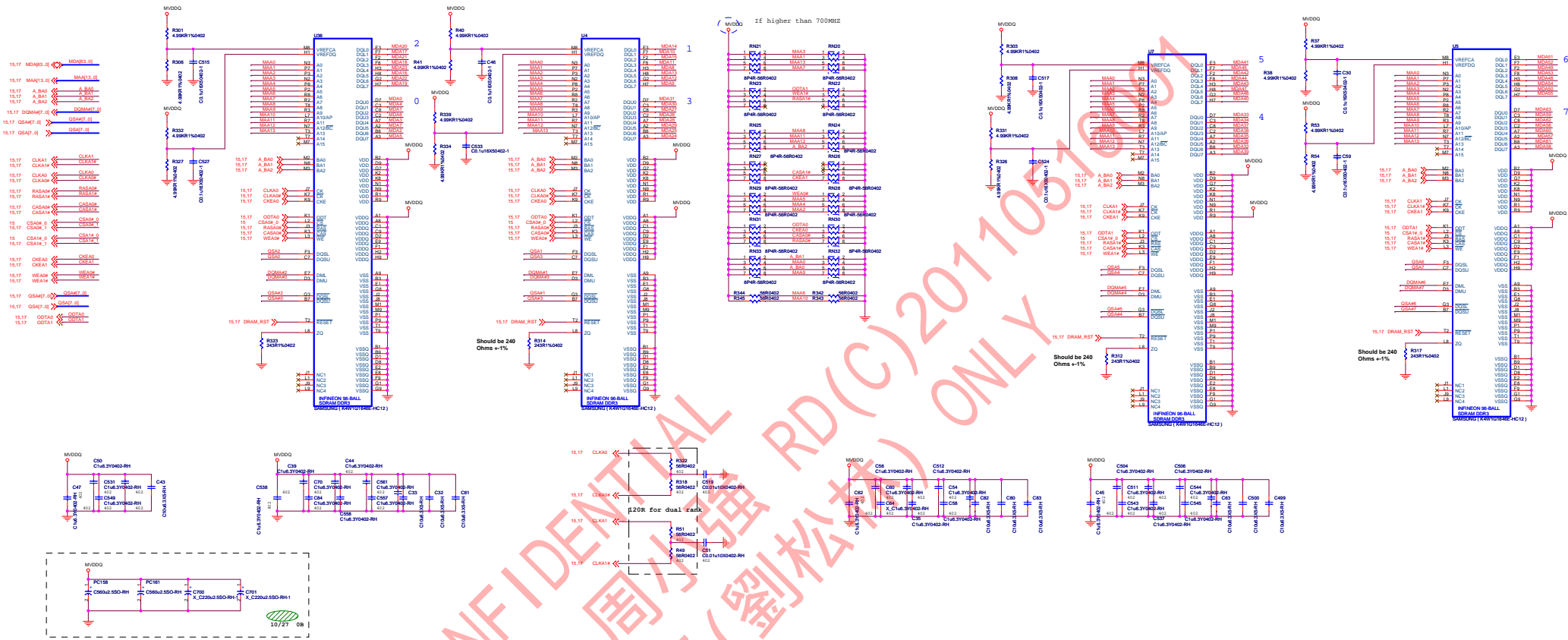
Title			
PARK-power straps			
Size	Document Number		Rev
Custom	MS-1688		1
Date:	Thursday, November 26, 2009		Sheet 14 of 52

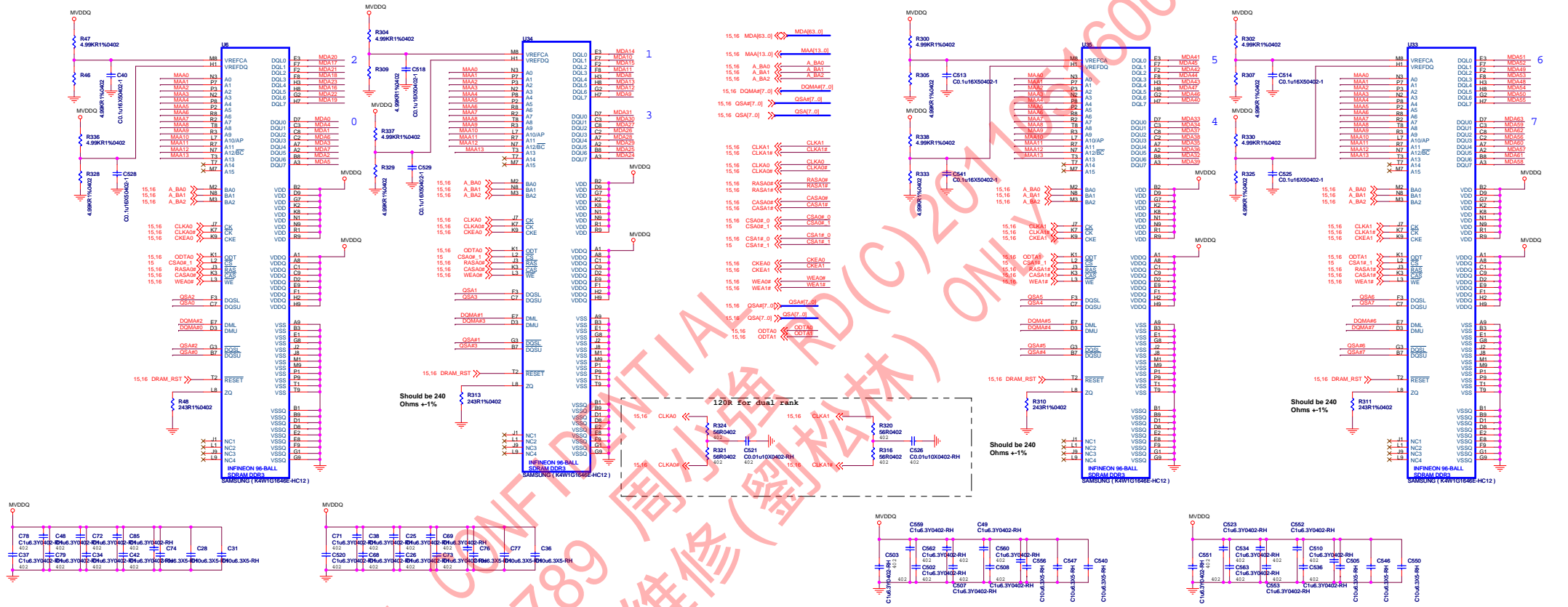
DIVIDER RESISTORS	DDR2 / DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R



MEMORY INTERFACE







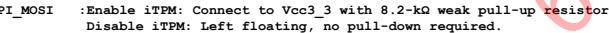
9/17

9/16 QS之後的 版本只要R481 上件(TCK)

TP_HDA_DOCK_EN# R581 1KR0402 >> BIOS_LOCK 30

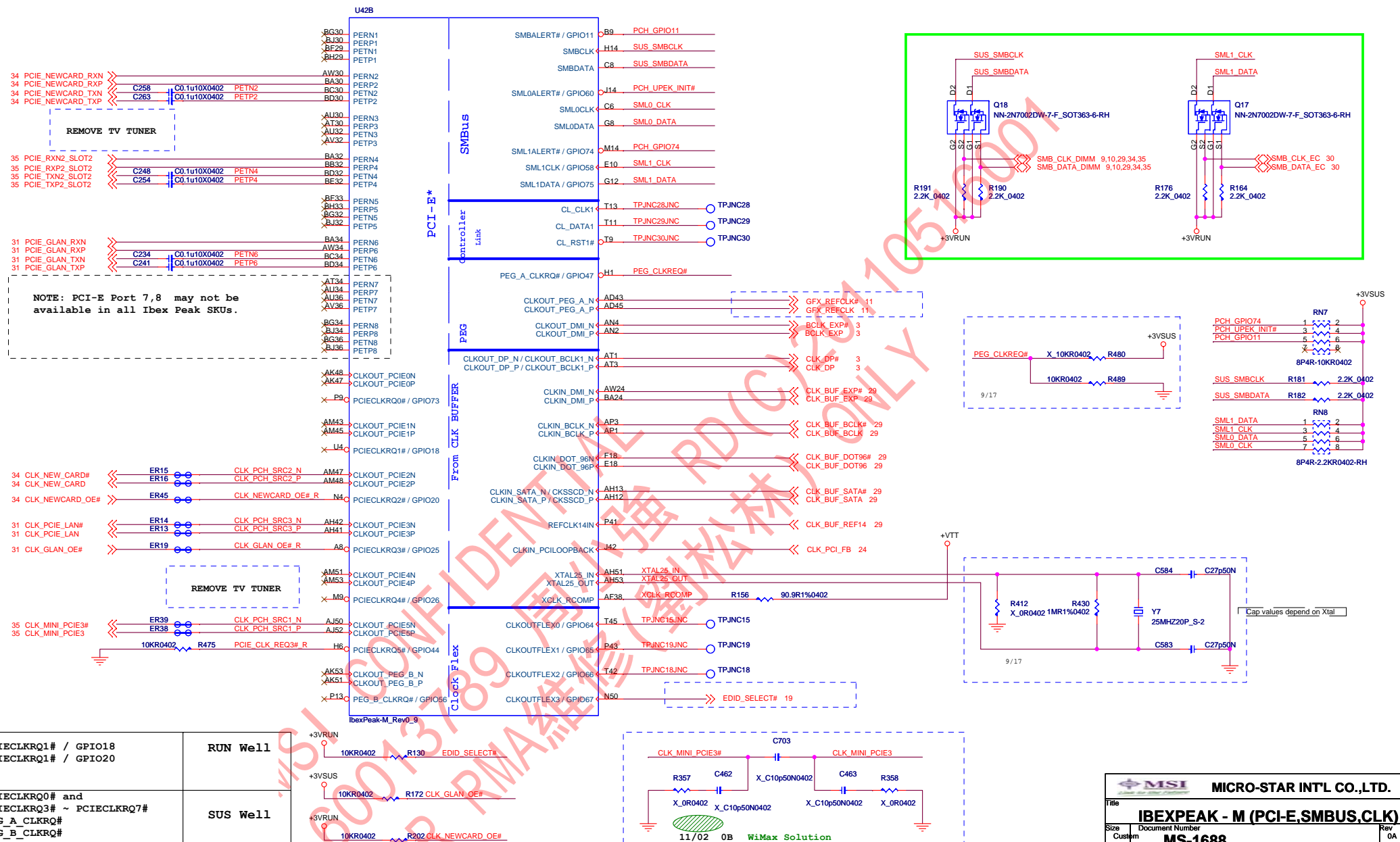
R159 X_1KR1%0402 0B

10/27 0B stuff can override SPI flash (ME code)



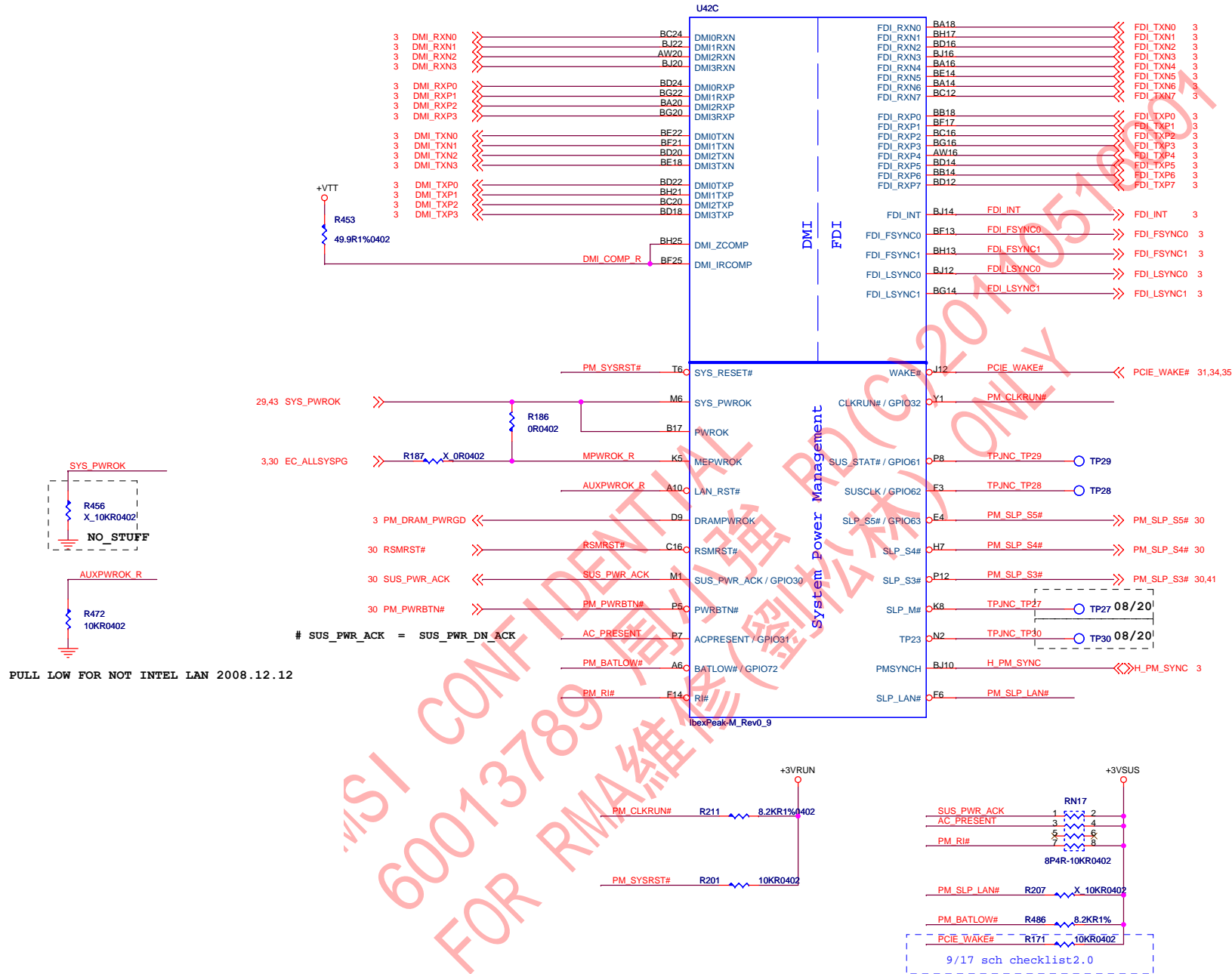
Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

IBEXPEAK - M (PCI-E, SMBUS, CLK)

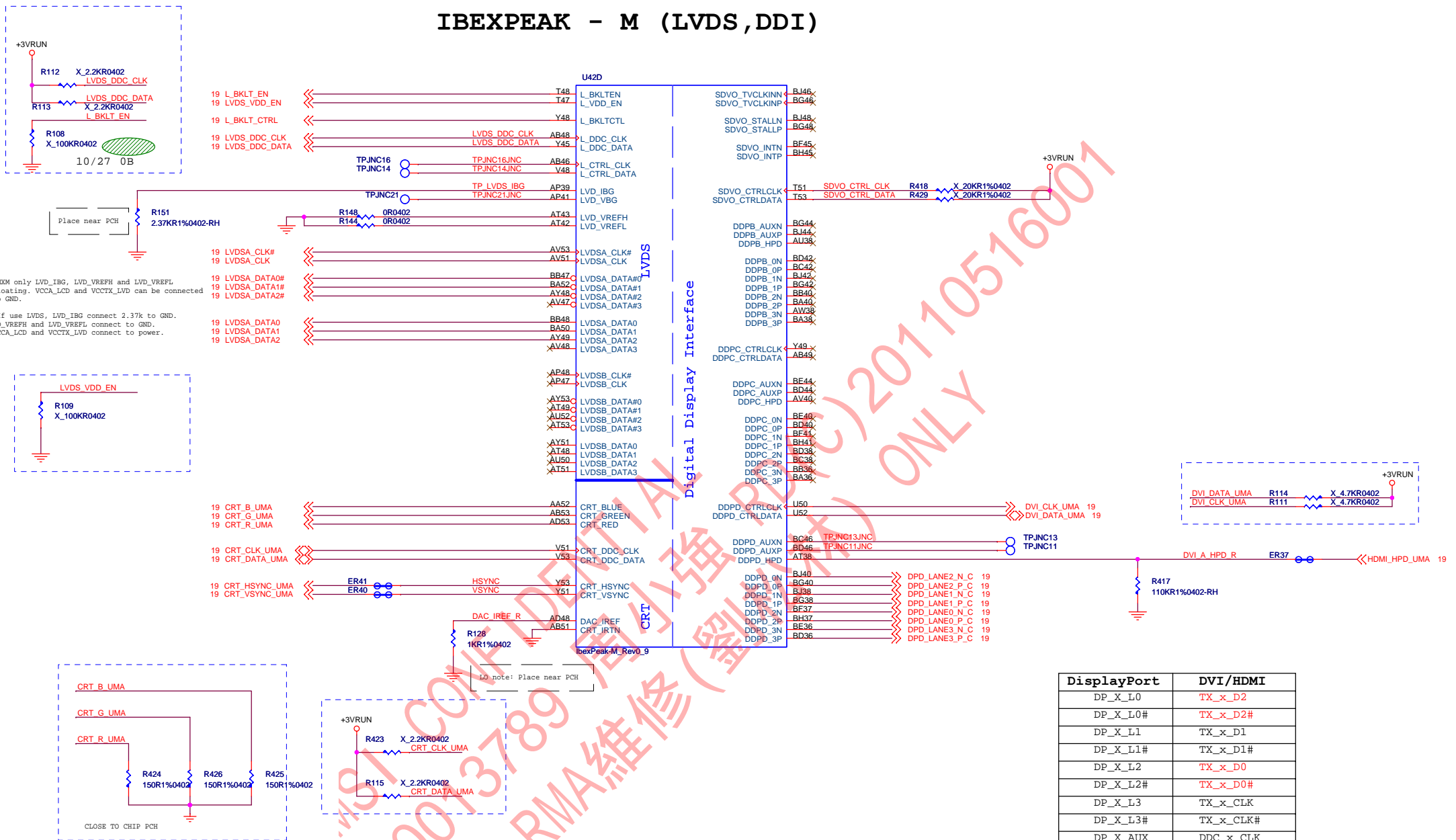


PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

IBEXPEAK - M (DMI, FDI, GPIO)



IBEXPEAK - M (LVDS,DDI)

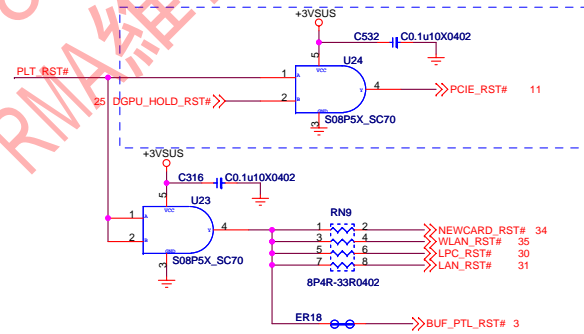
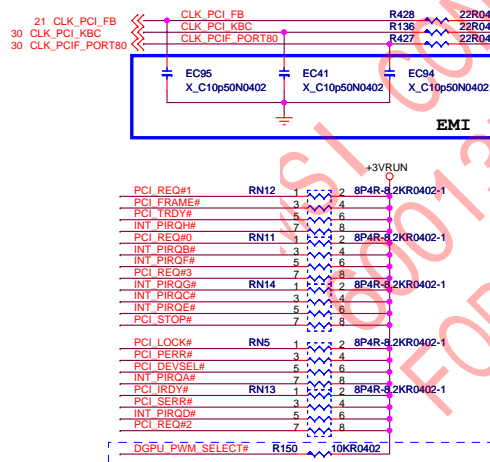
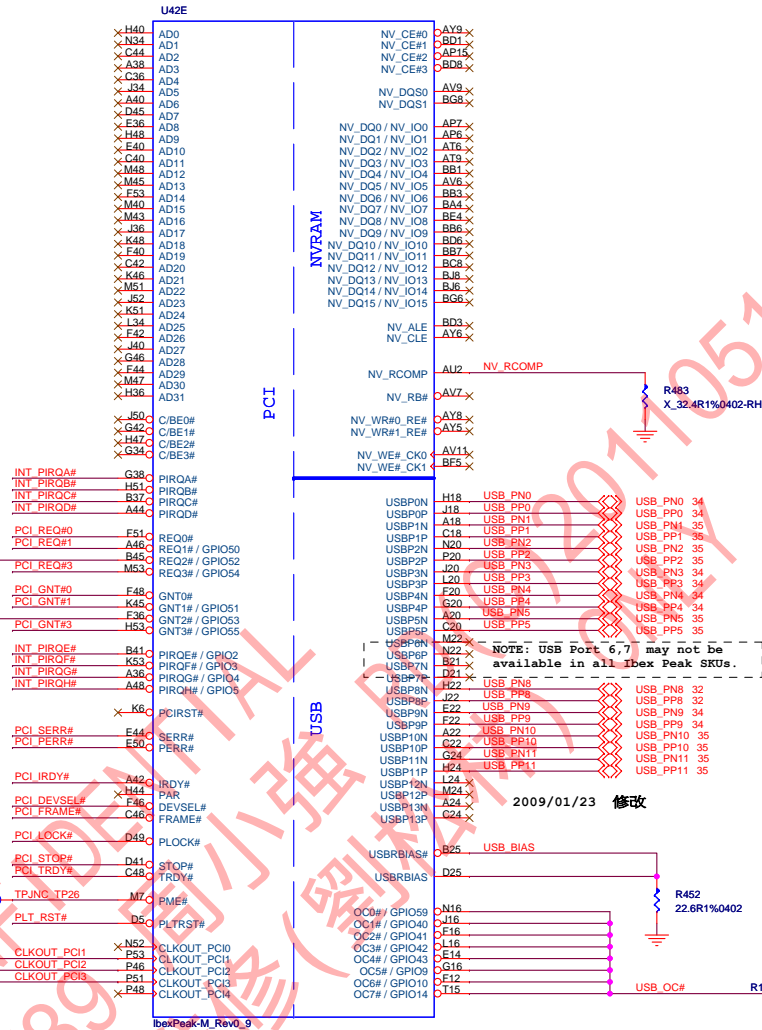
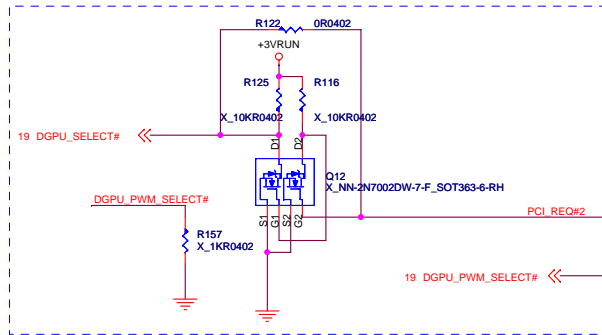
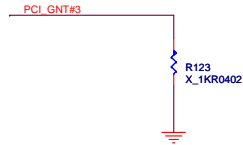
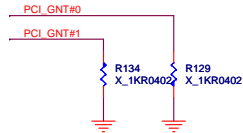


DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

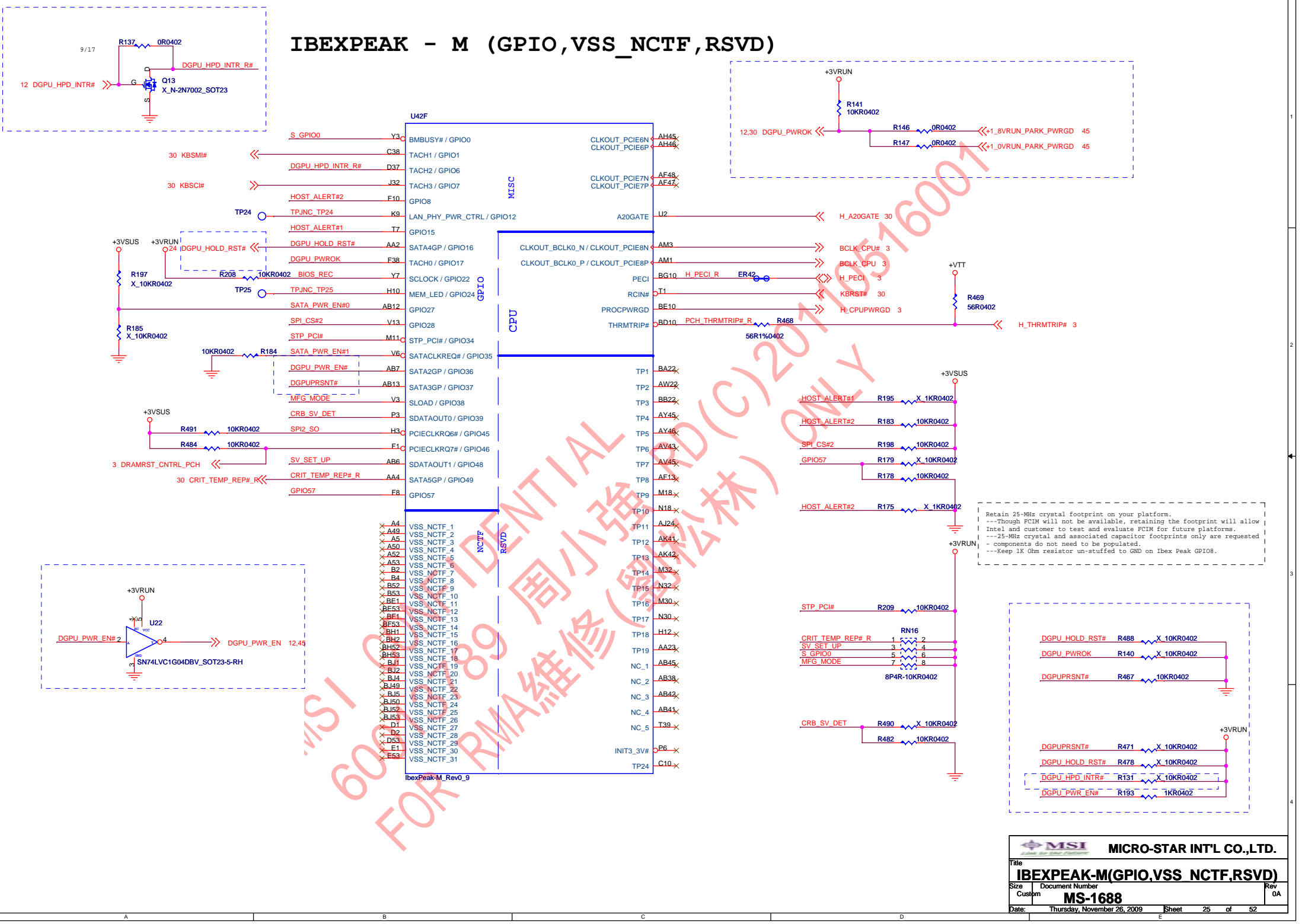
IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

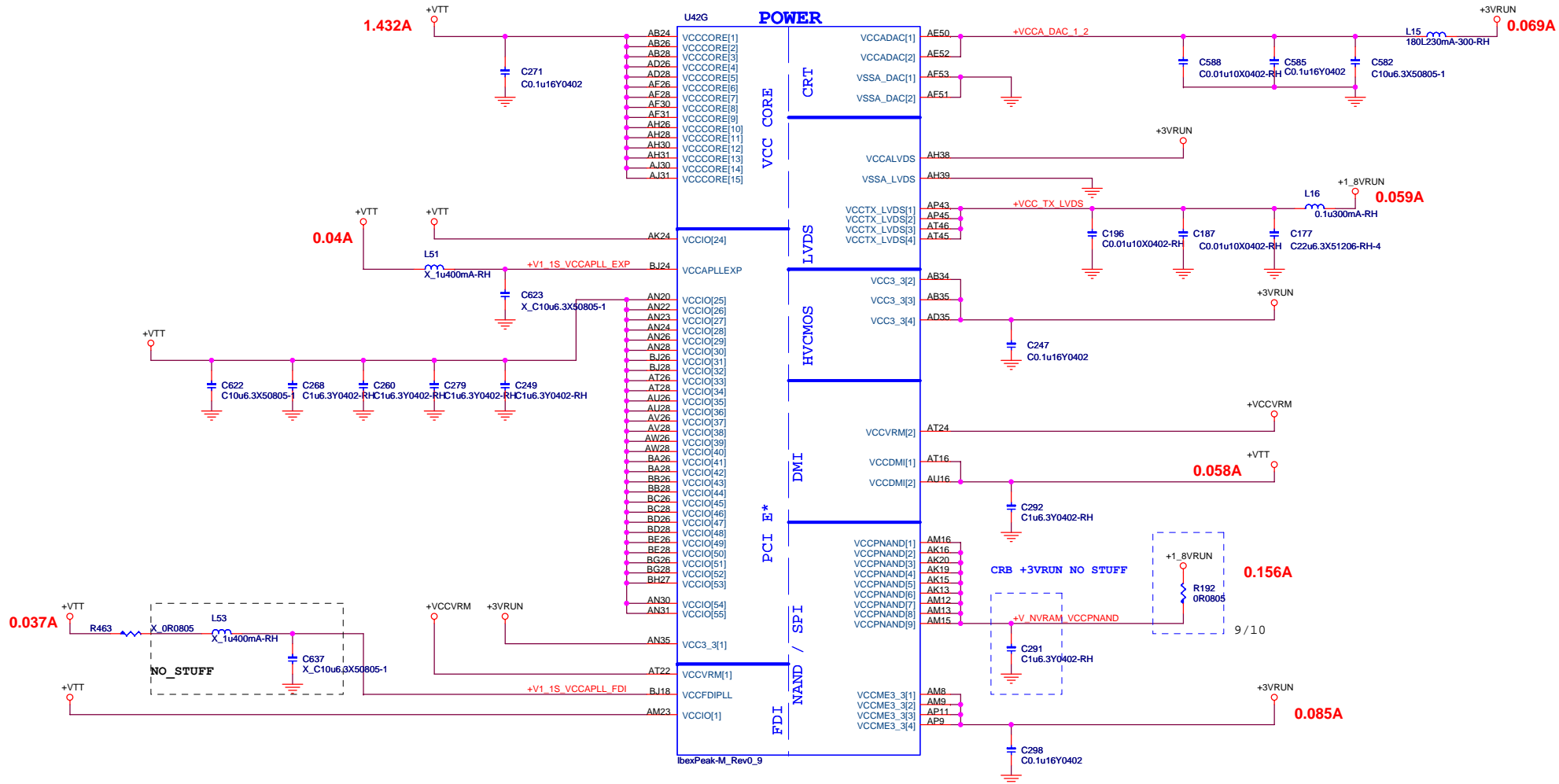
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



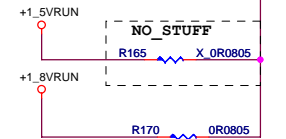
IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

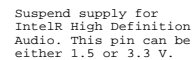


IBEXPEAK - M (POWER)

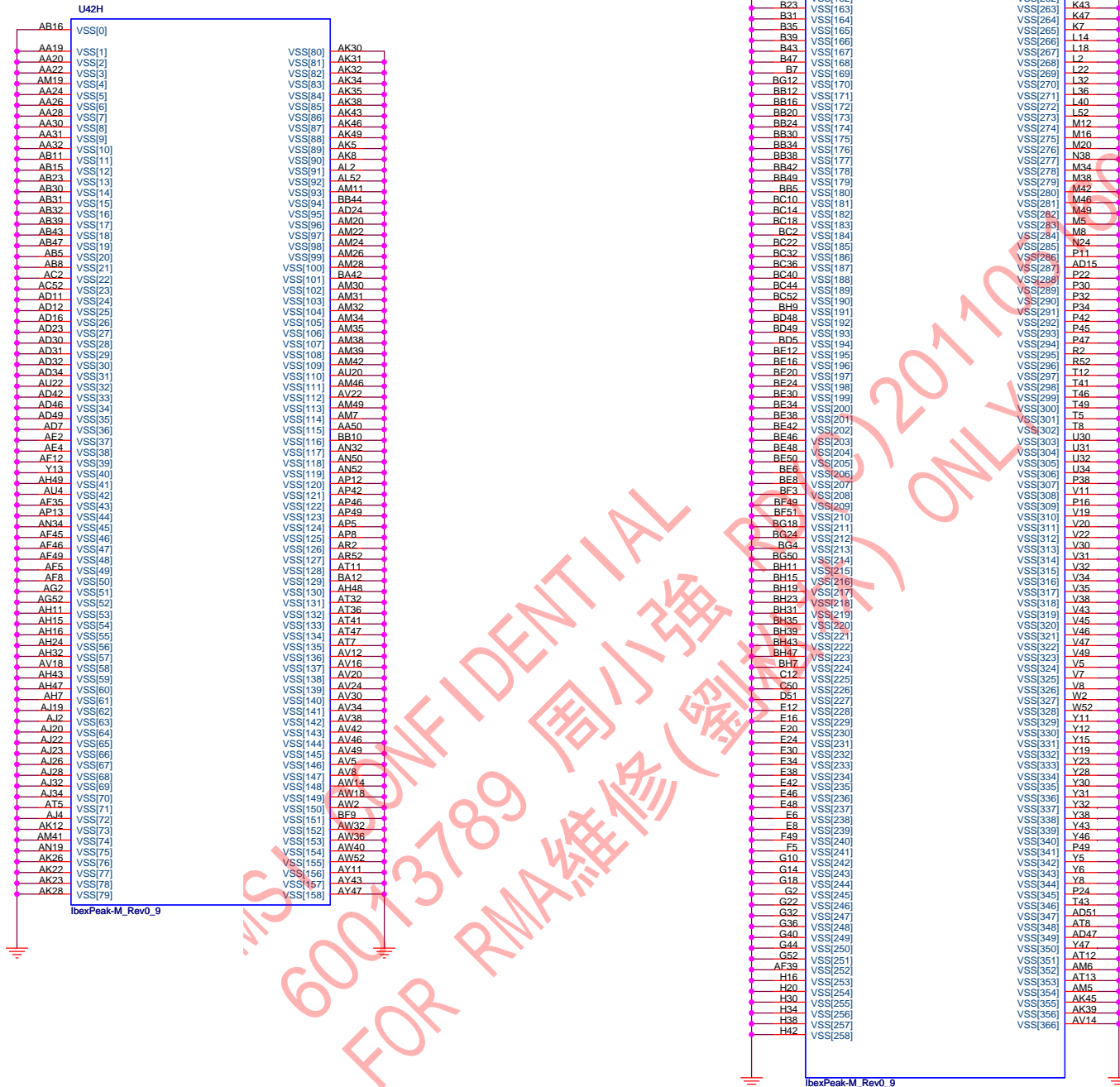


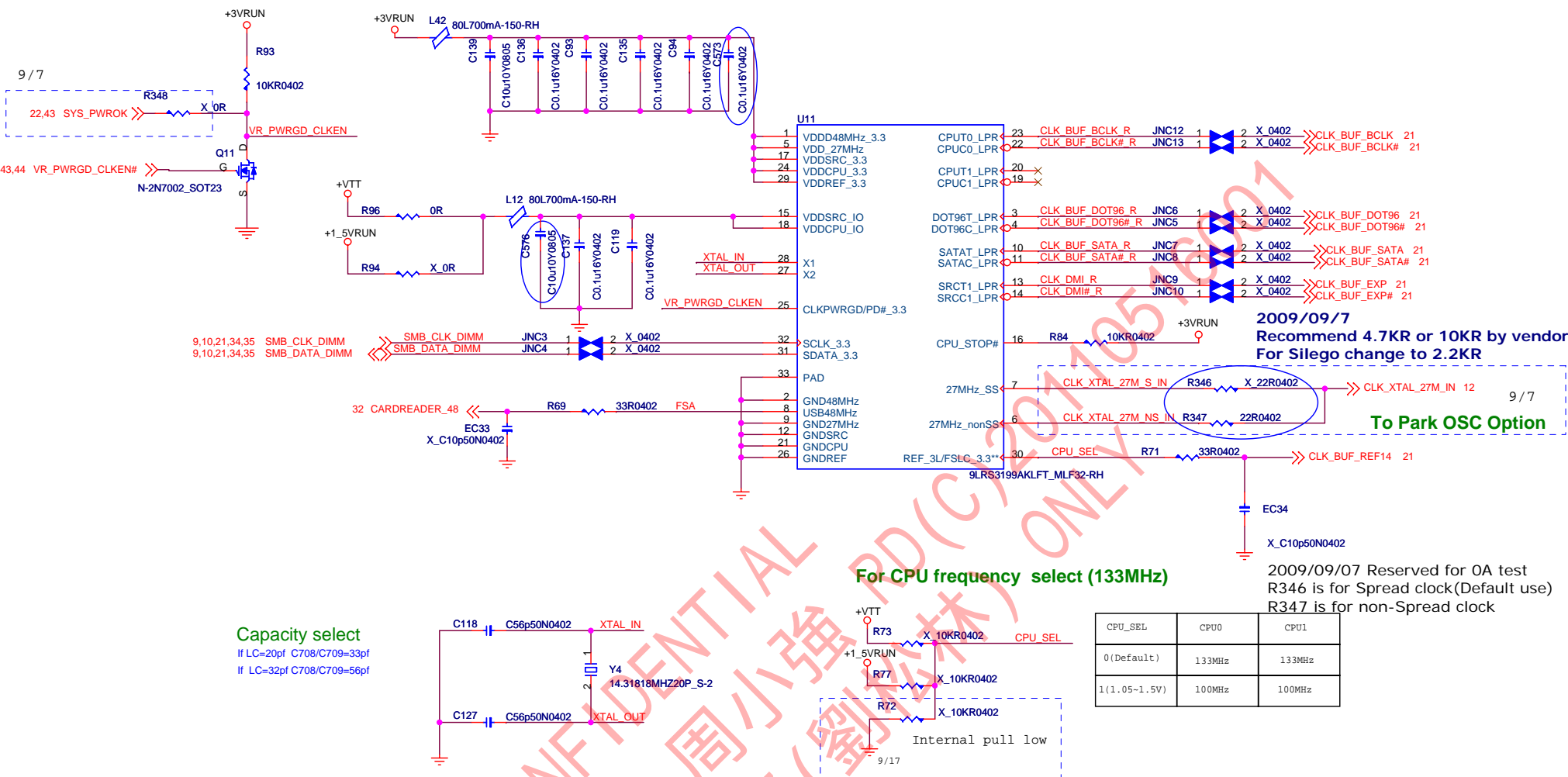
The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



IBEXPEAK - M (POWER)

IBEXPEAK - M (GND)





Capacity select
If LC=20pf C708/C709=33pf
If LC=32pf C708/C709=56pf

For CPU frequency select (133MHz)

2009/09/7
Recommend 4.7KR or 10KR by vendor
For Silego change to 2.2KR

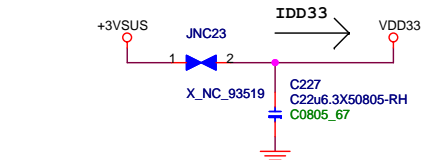
To Park OSC Option

CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

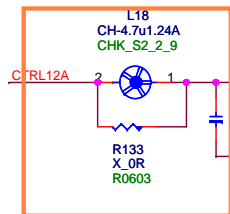
Co-Lay Note:

For IDT IC91RS3199
R84,R73,R71=10Kohm

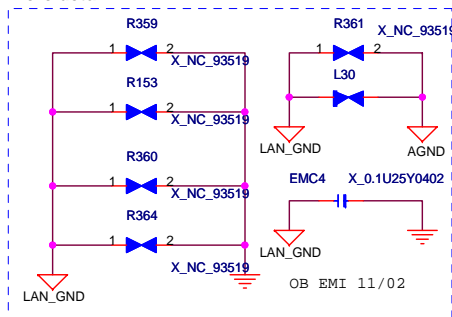
For Silego SLG8SP587
R84,R73,R600=4.7Kohm



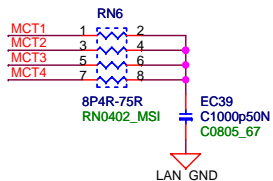
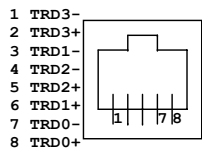
$$\begin{aligned} \text{IDD33} &= \text{Icc33} + \text{ICCL2} \\ &= 58\text{mA} + 289\text{mA} \\ &= 347\text{mA} \end{aligned}$$



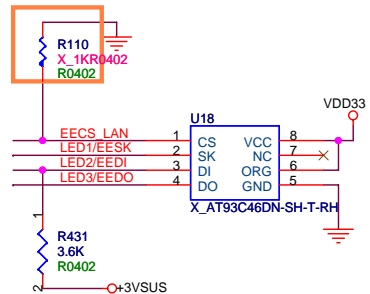
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C171 and C181 to L18 must be within 0.5cm. Refer to Layout guide for more detail.



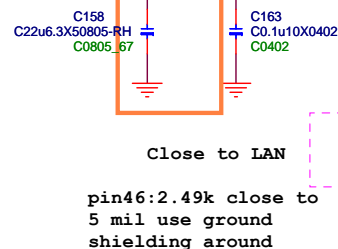
RJ45 Pin define



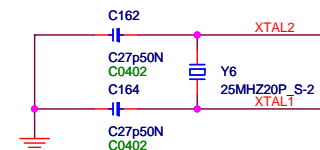
R110 is only required by RTL8102EL



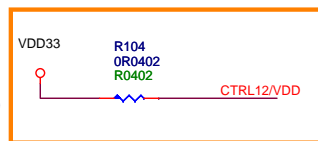
C158 is only RTL8111DL



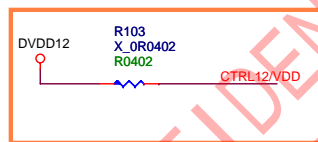
R106 is only RTL8111DL



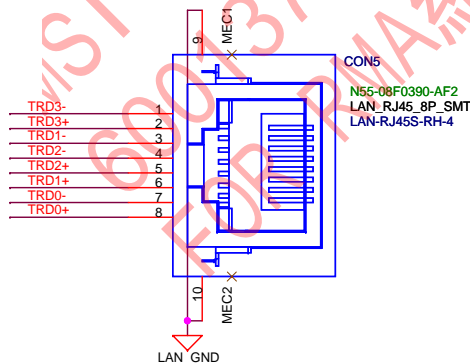
For RTL8111DL, use this block



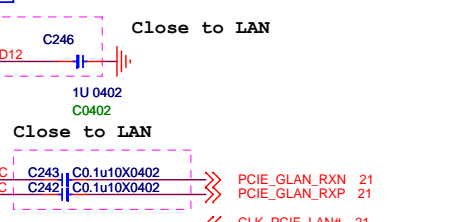
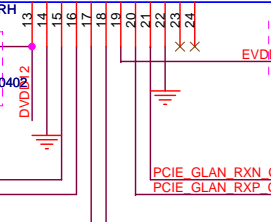
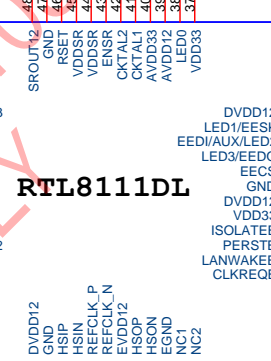
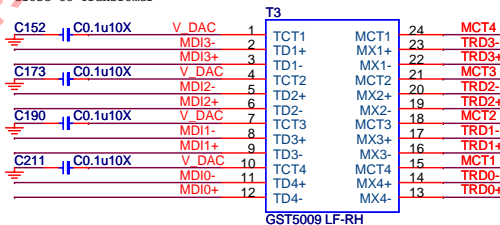
For RTL8102EL/8103EL, use this block

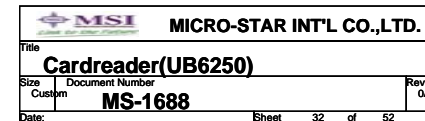


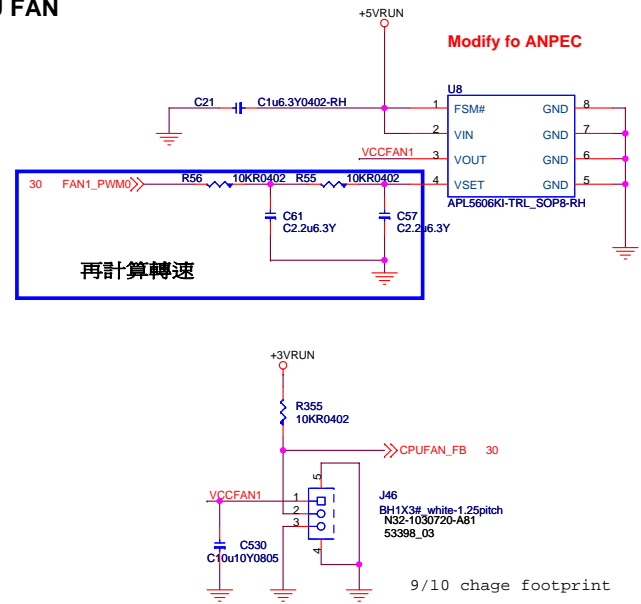
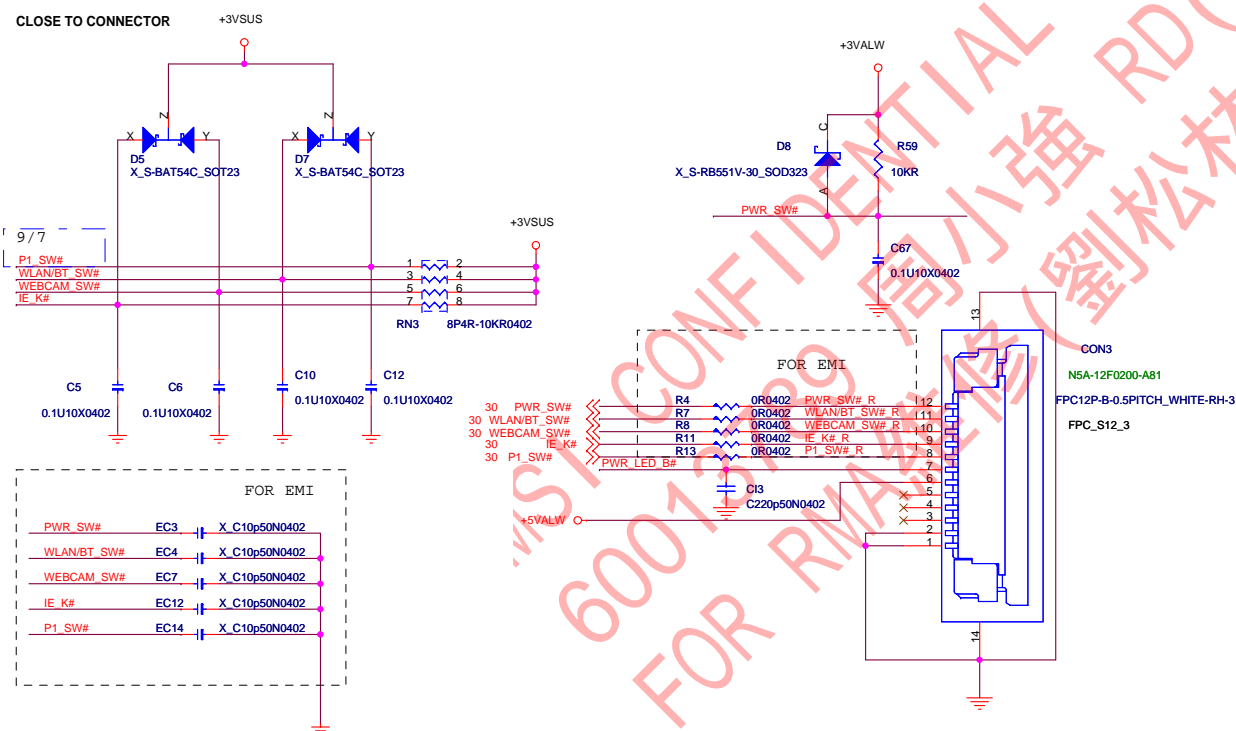
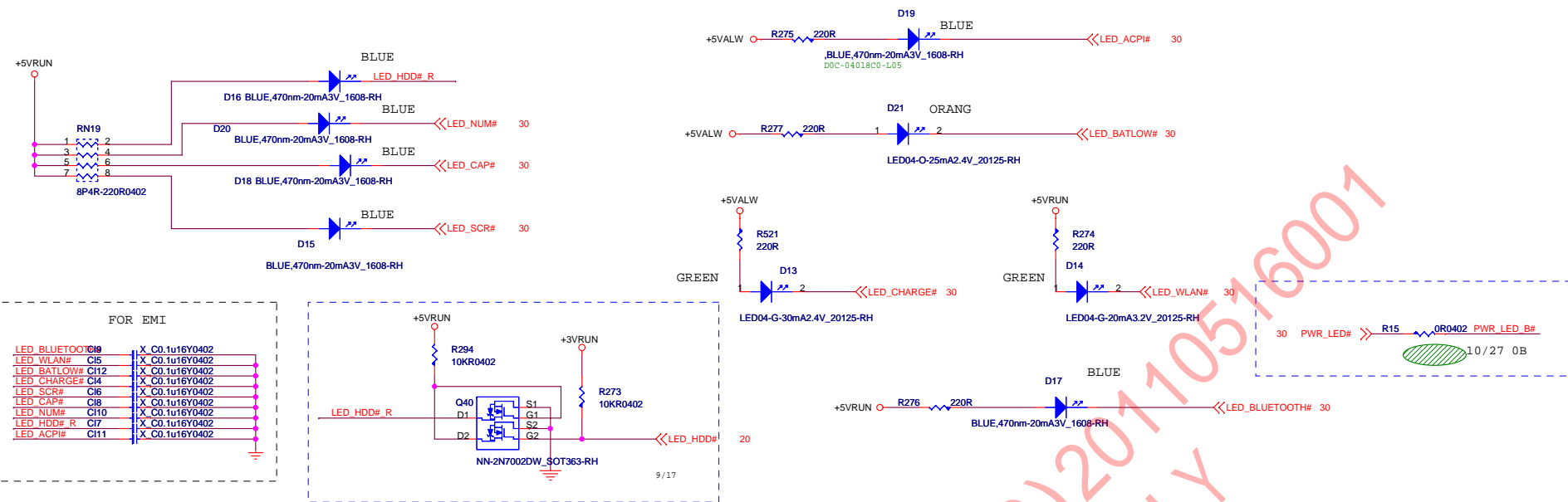
Close to Transformer



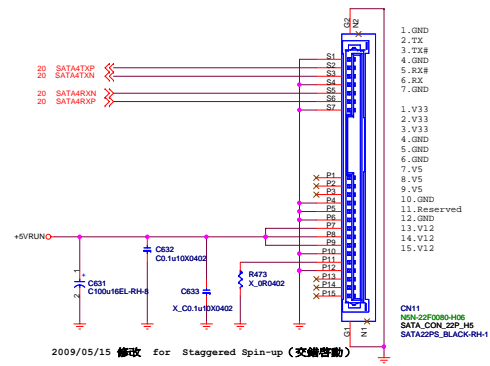
LAN MAGNETICS



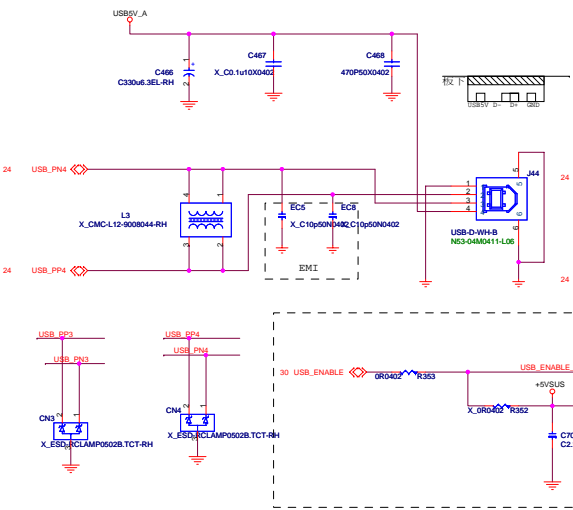




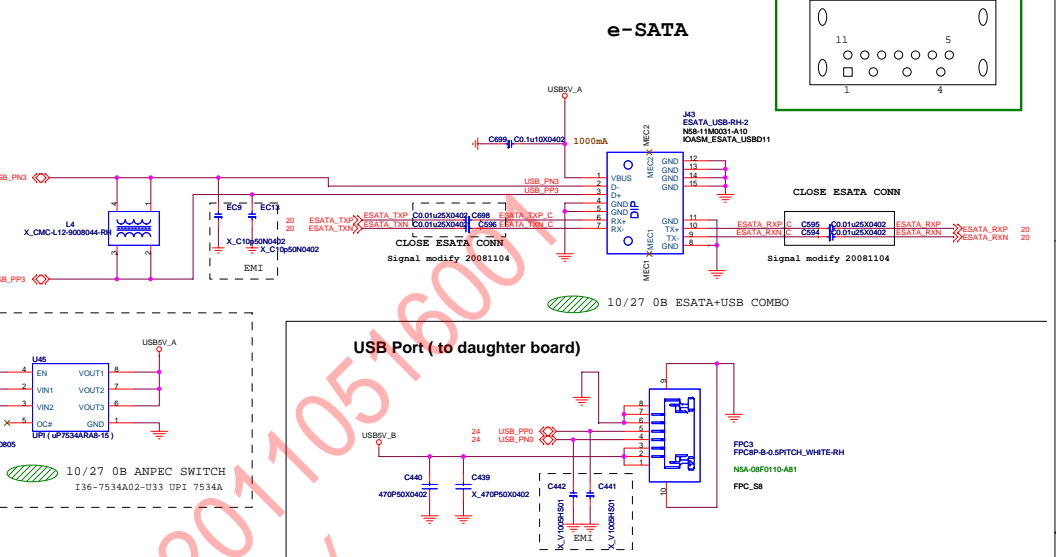
SATA HDD



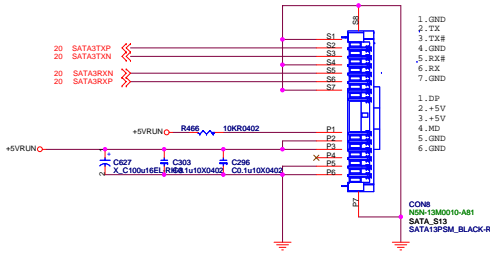
USB Port



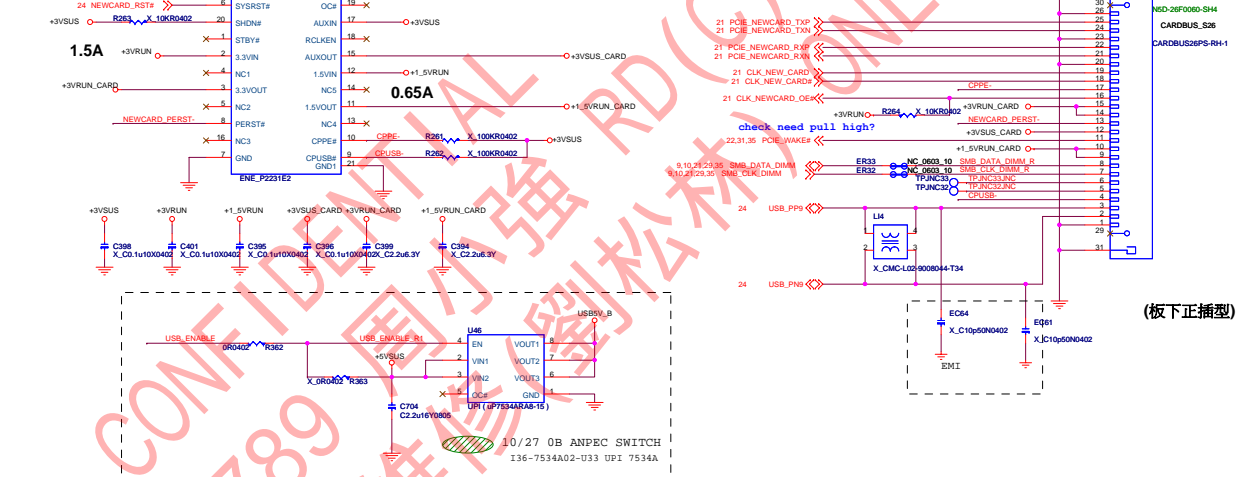
e-SATA



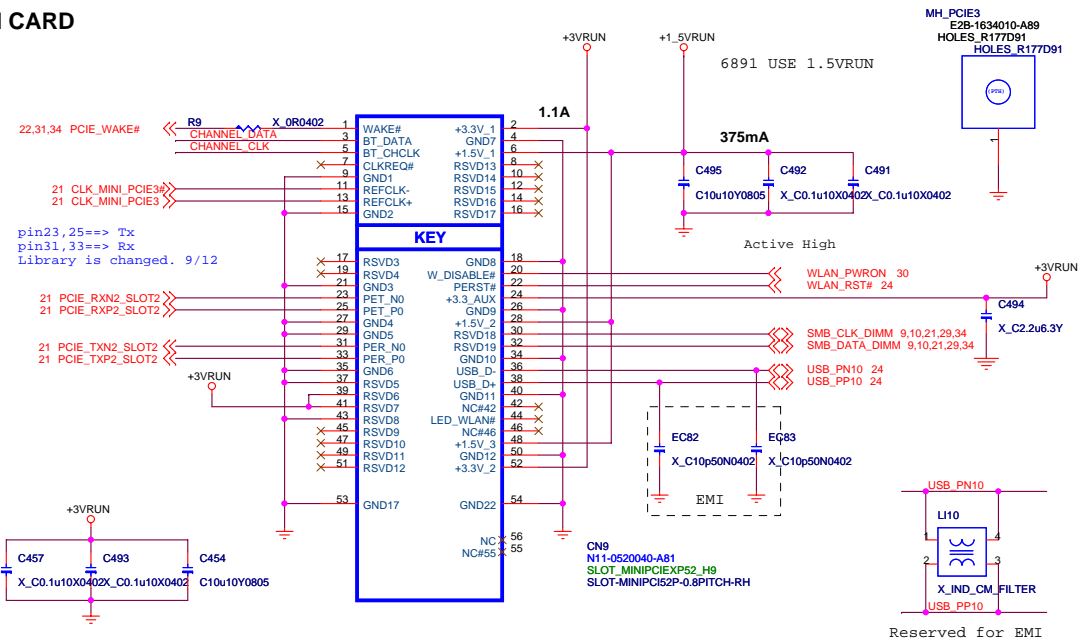
SATA ODD



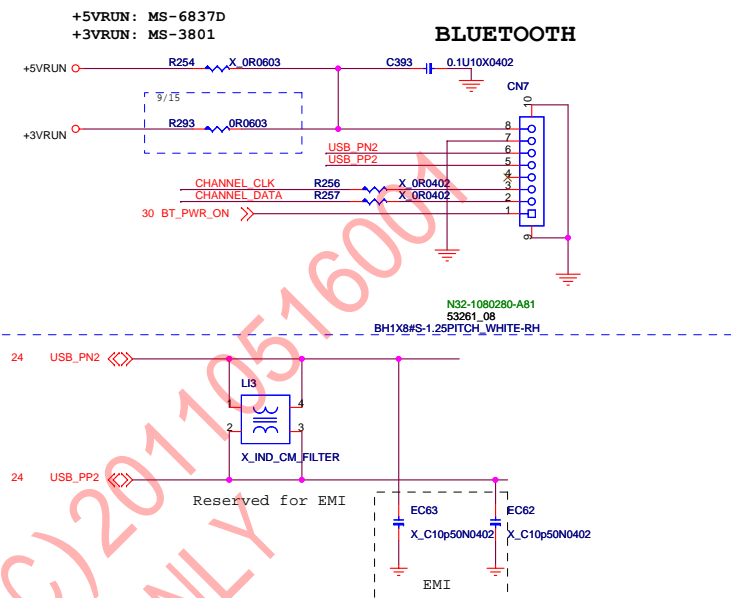
NEW CARD



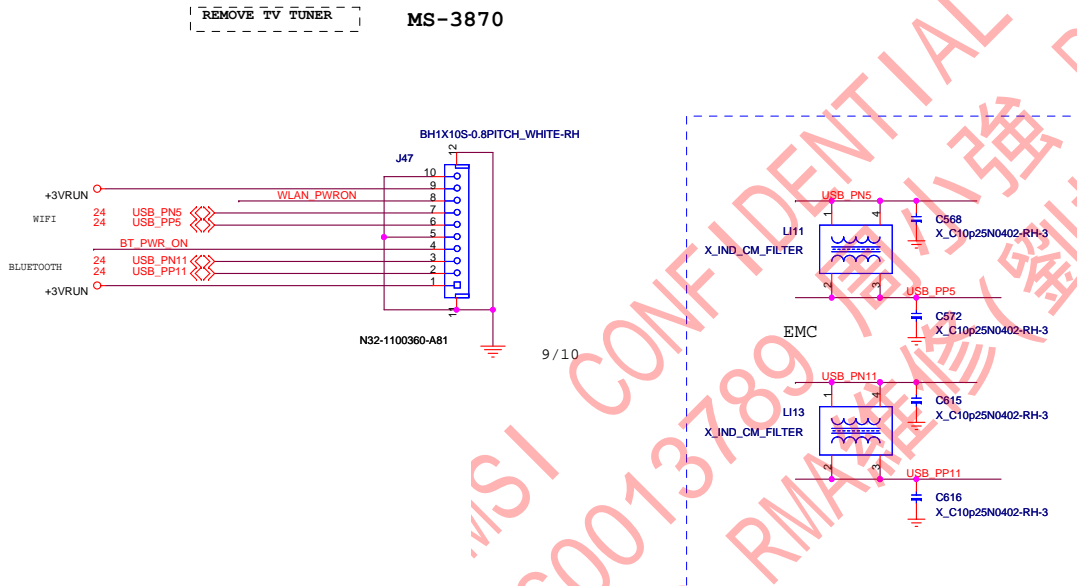
WLAN CARD



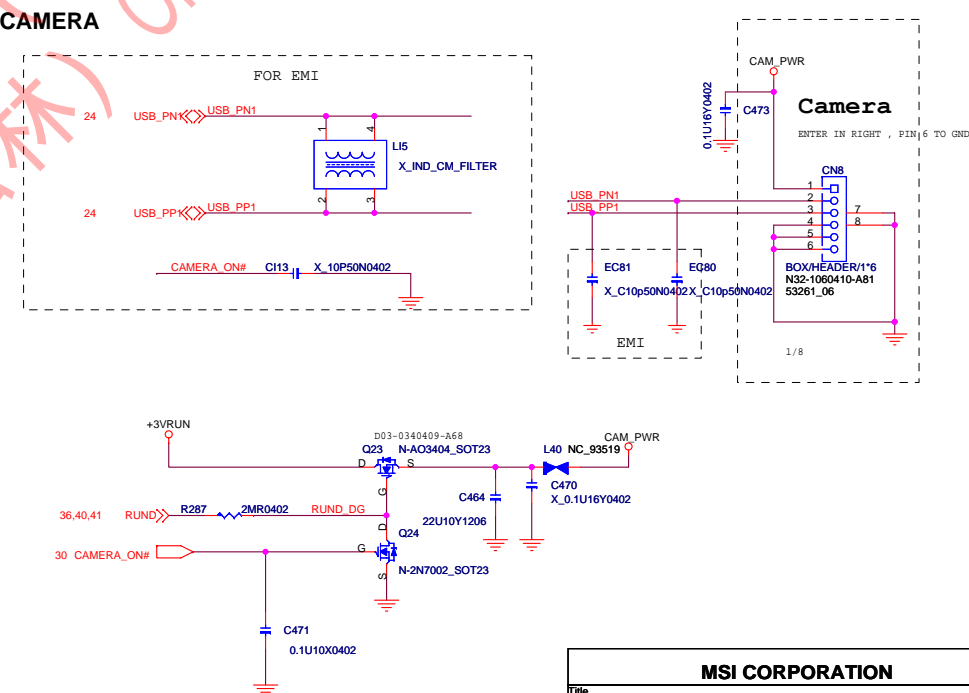
BLUETOOTH

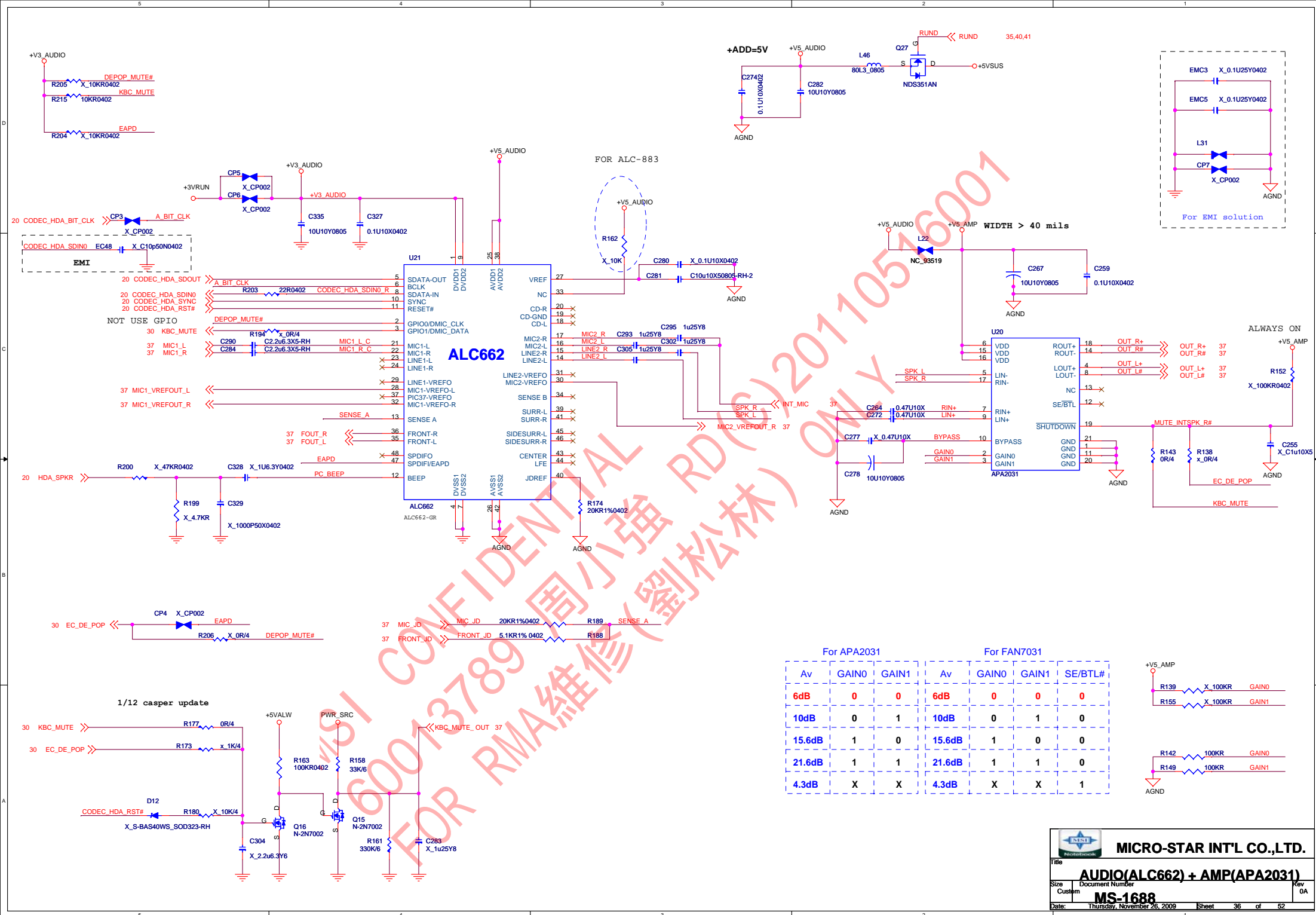


MS-3870

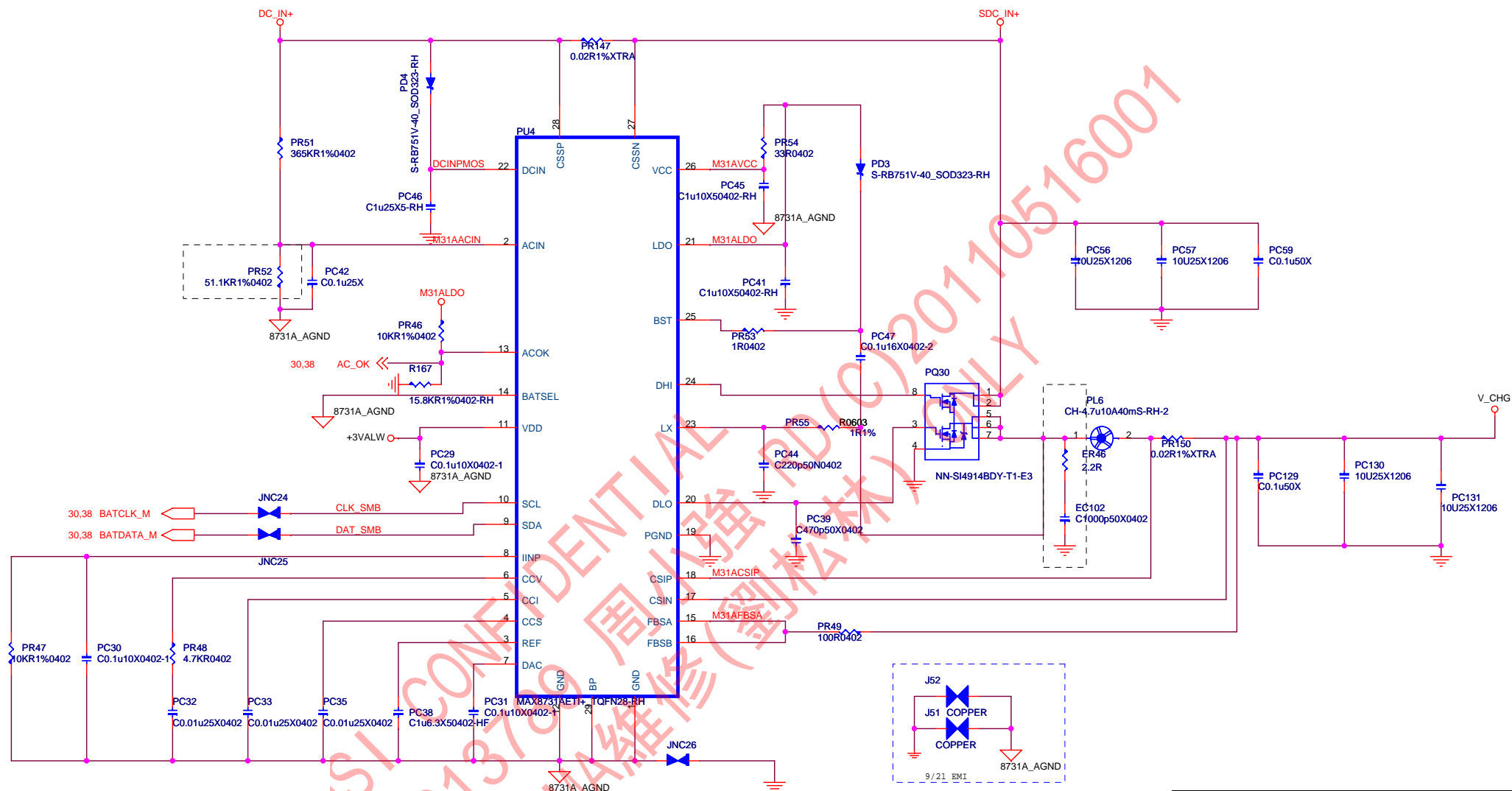


CAMERA






Adapter input voltage set 19 Voltage



IINP :
 1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
 2. $V_IINP = IINPUT \times RS1 \times 3mA/V \times PR25$

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$$I_{LIM} = (R_{imax} \times 20\mu A / R_{dson}) + 1.82A$$

Vlot=1.515V


OCF 19A
MAX 14A

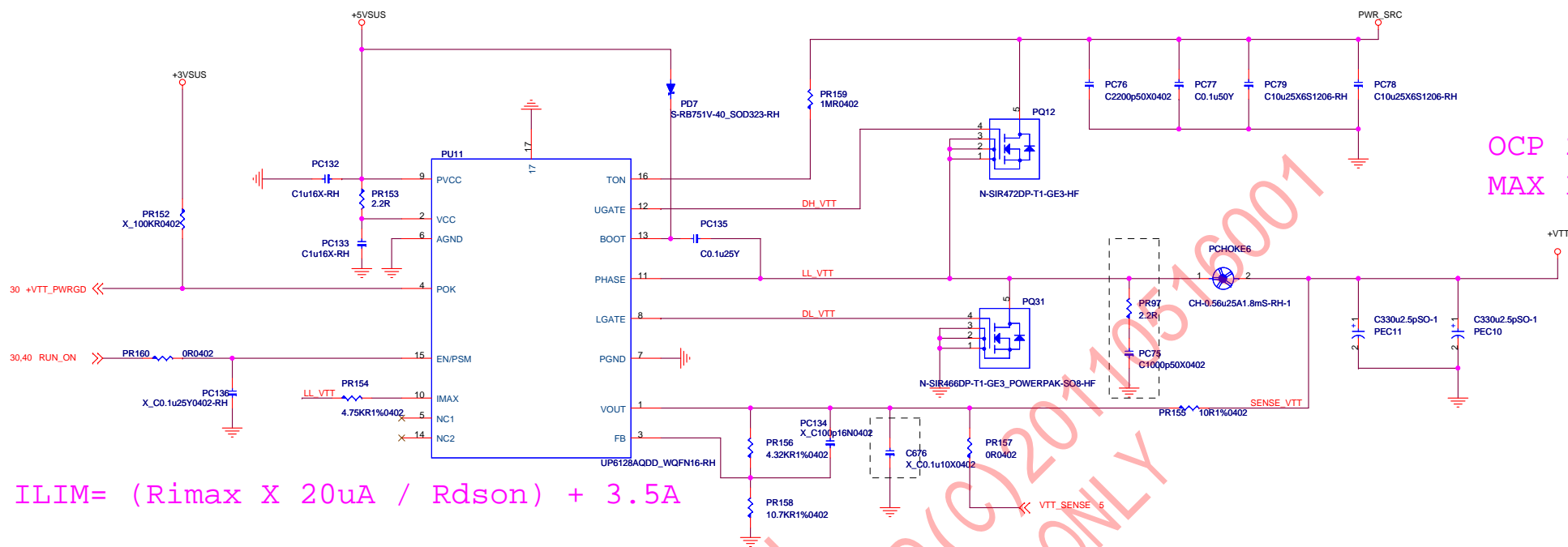
MAX 2A

8

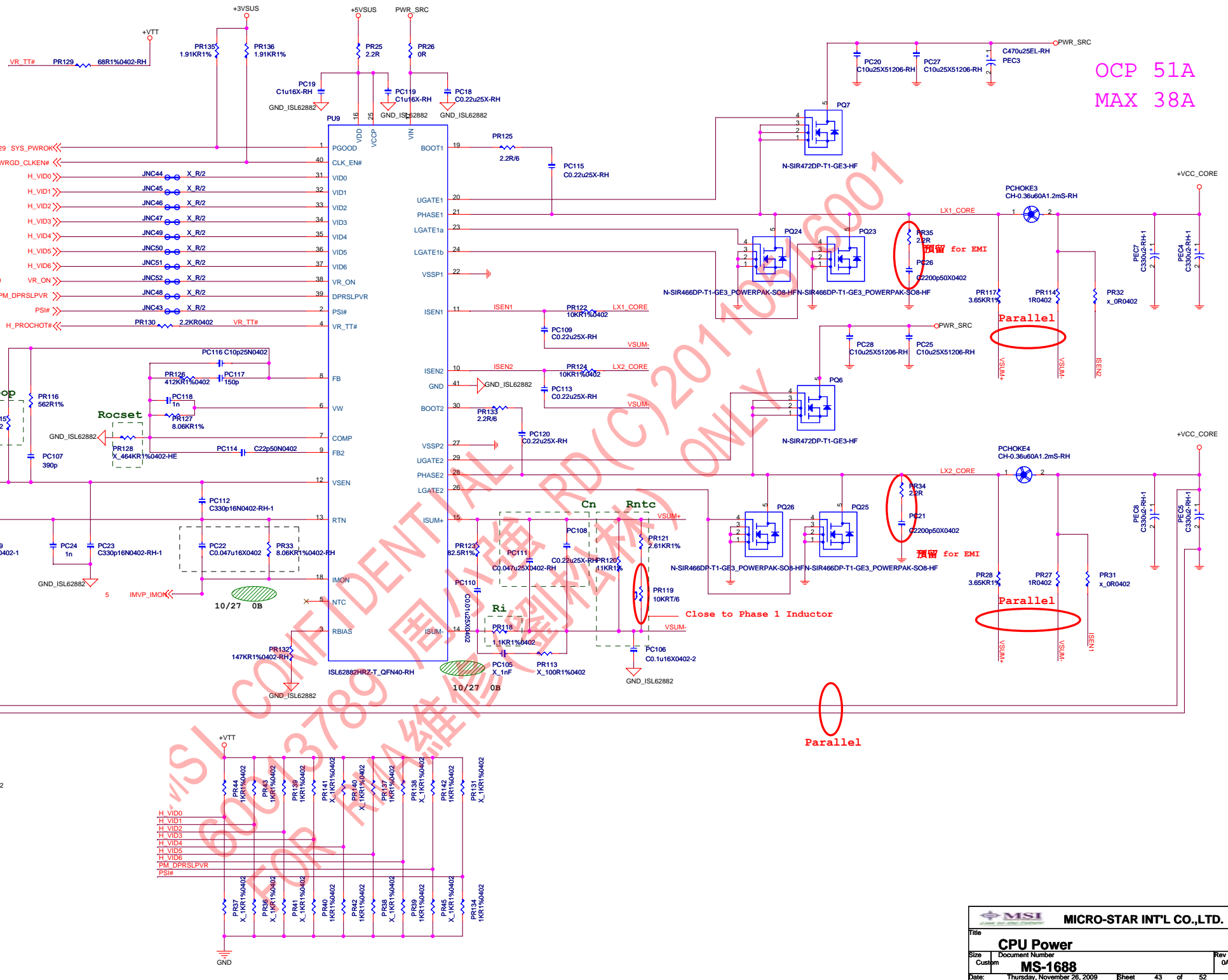
1

2

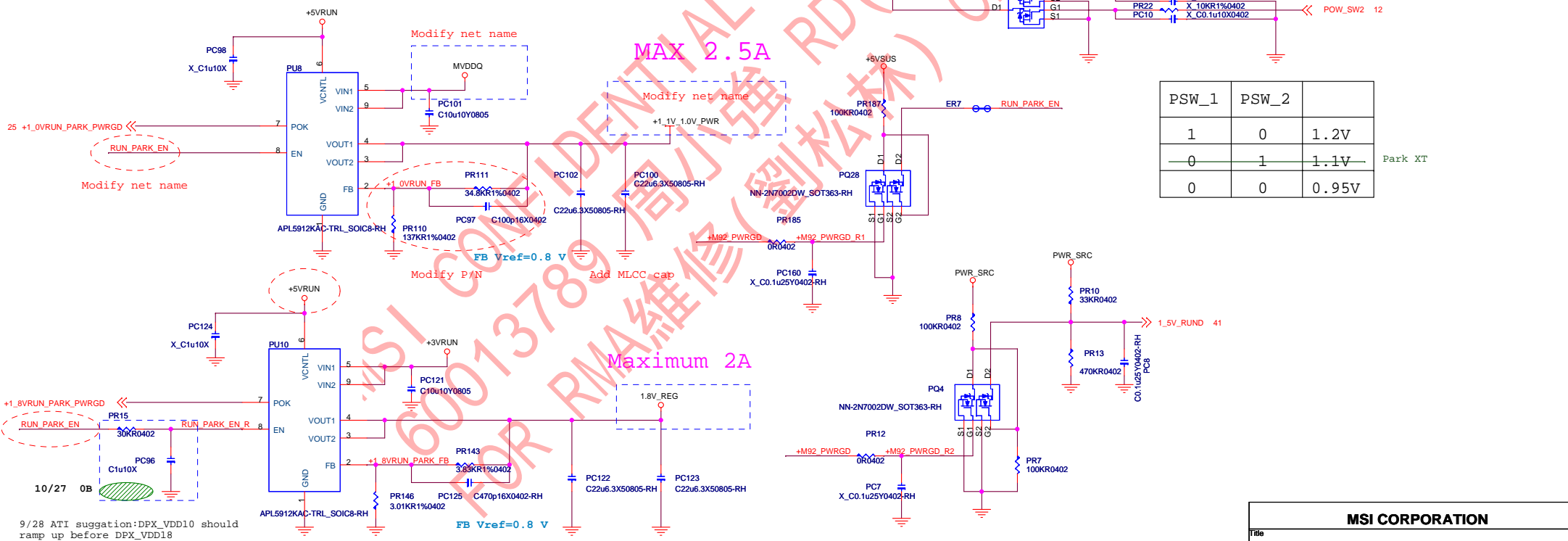
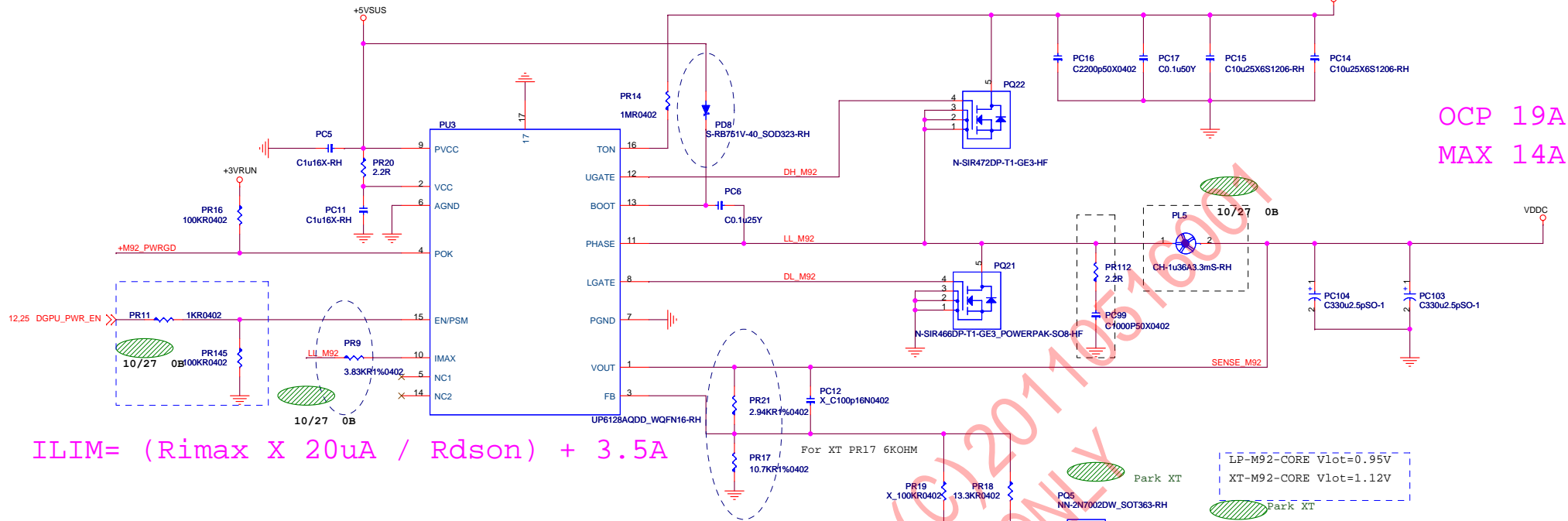
 MICRO-STAR INT'L CO.,LTD.			
Title SMDDR VTERM /1 5VRUN			
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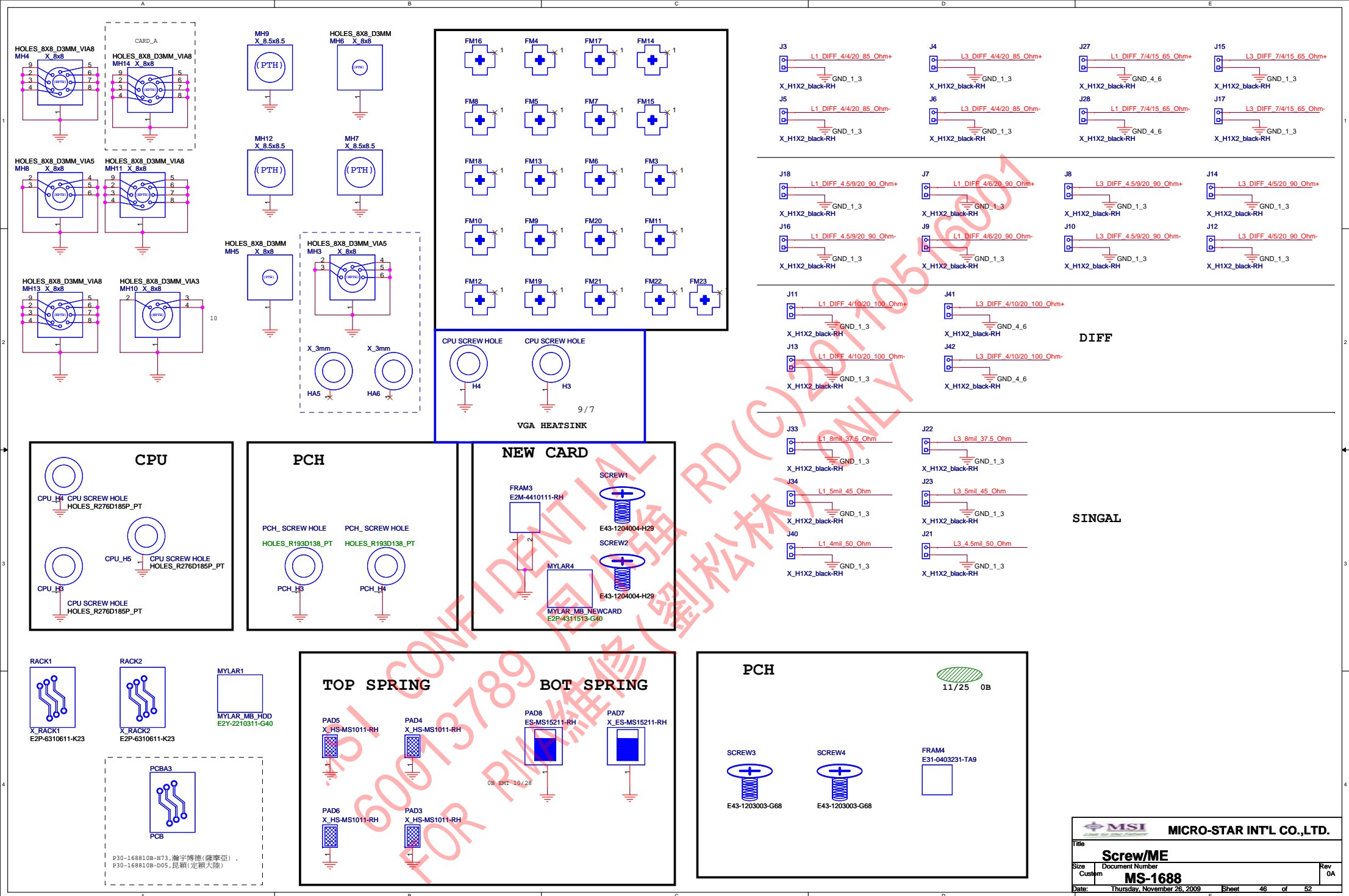


MSI MICRO-STAR INT'L CO.,LTD.			
Title			
VTT Power, +1.8VRUN			
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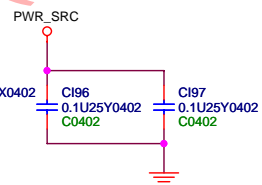
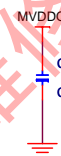
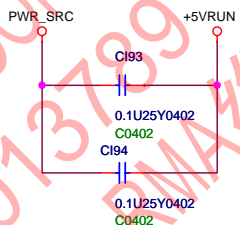
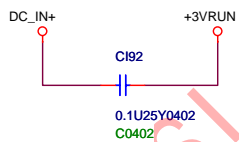
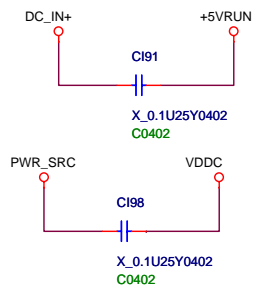
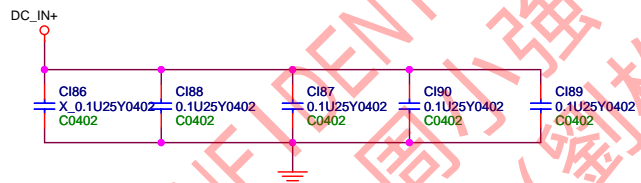
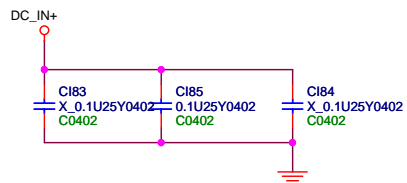
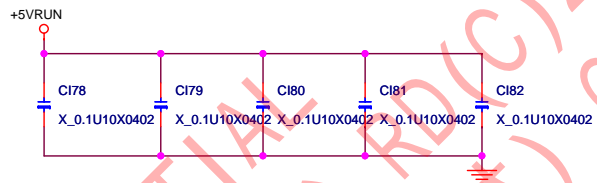
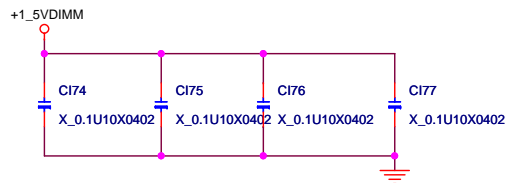
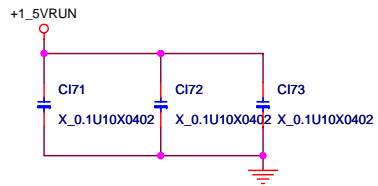
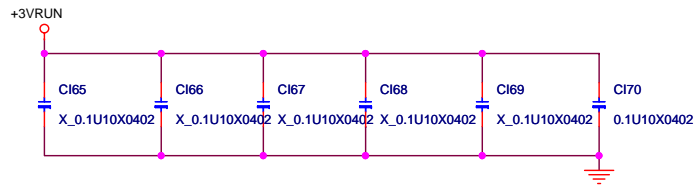
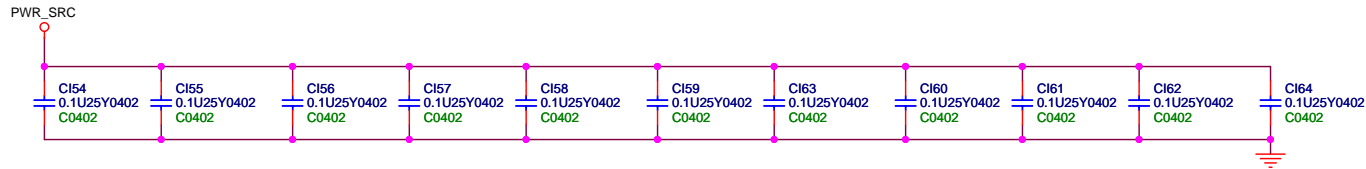
OCP 51A
MAX 38A






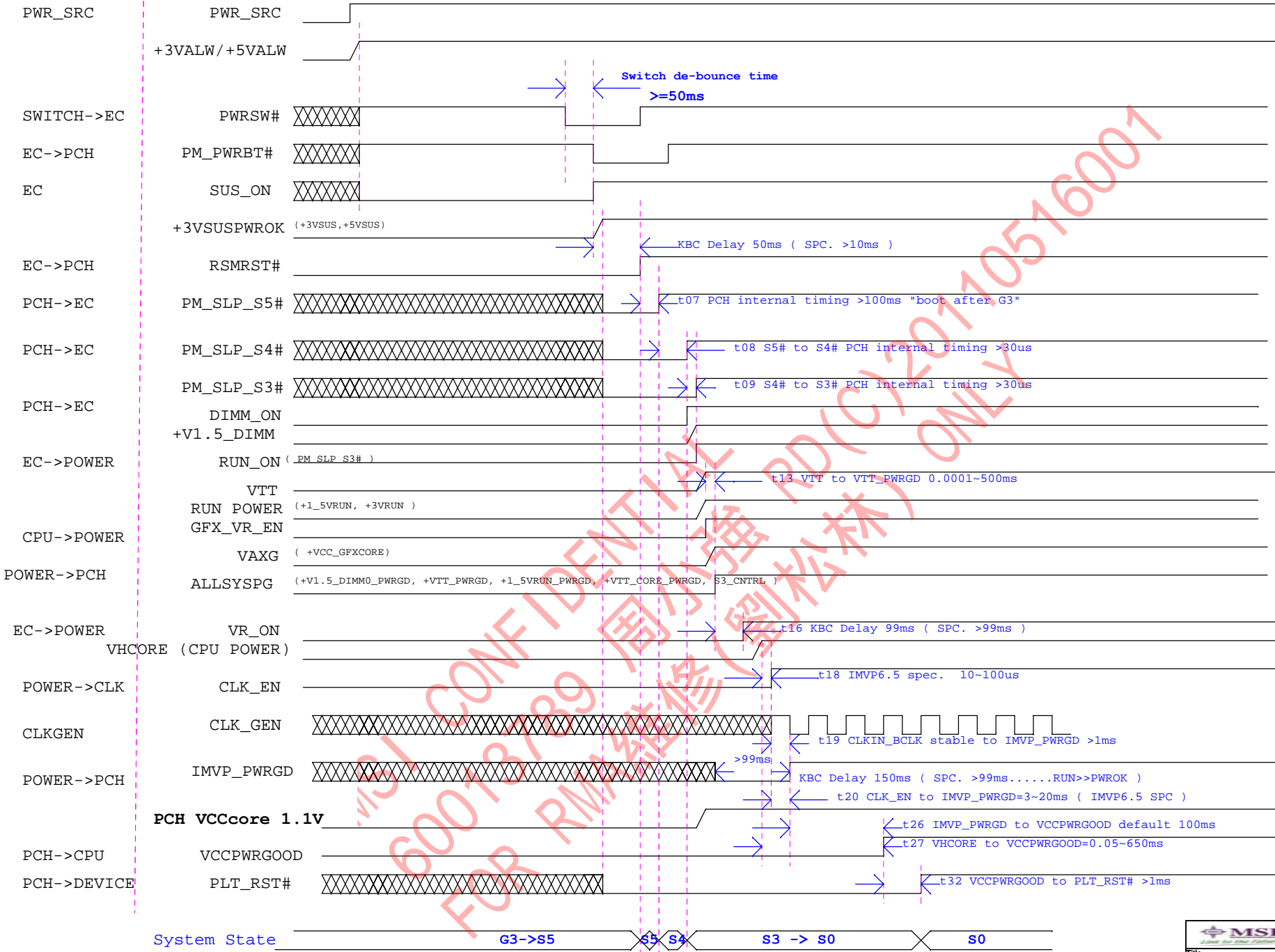
DIFF

SINGAL

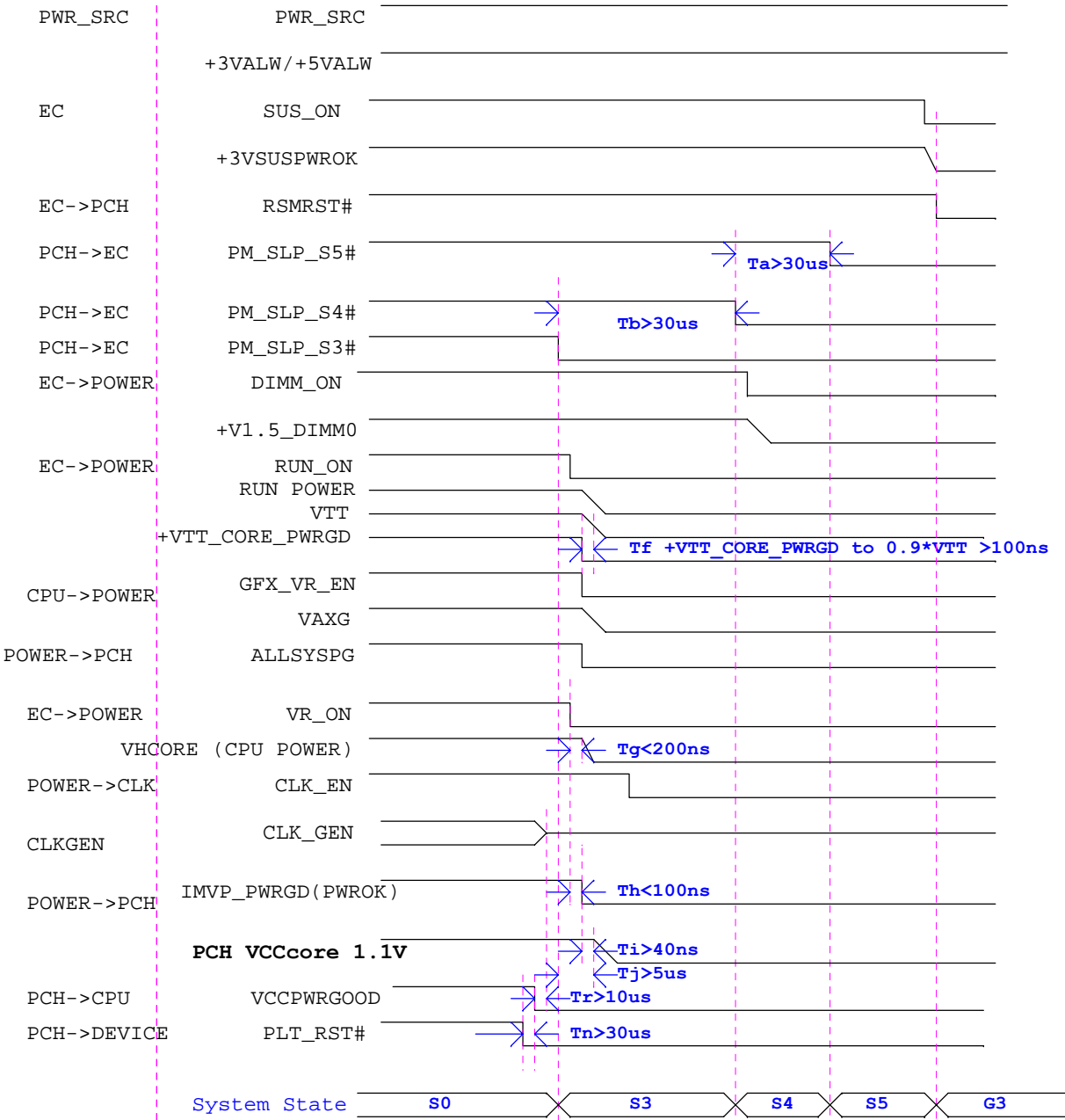


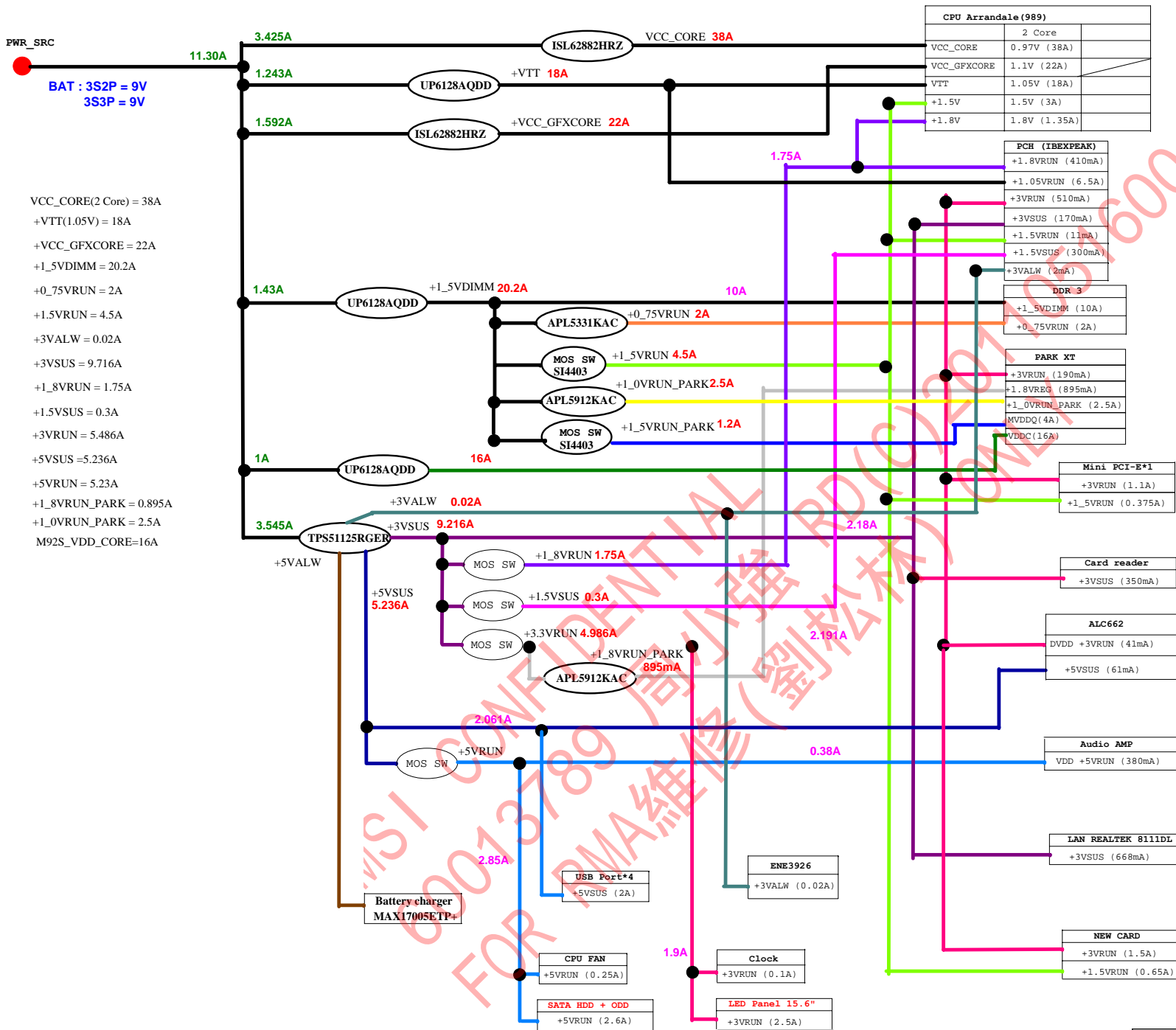
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Calpella System Power on Sequence DC mode



Power down Sequence DC mode S0 to G3





0B

- 1. Page 13, Add R354, R356 0 ohm for Park VDDR4 connection
- 2. Page 14, Stuff R92 10K ohms for GPIO12 straps
- 3. Page 15, Remove R50, R315
- 4. Page 18, Change L33~35 for CRT RGB
- 5. Page 19, Change D4 to BAS40 for HDMI testing
- 6. Page 20, Remove BIOS1 socket
- 7. Page 20, Add R581 1K ohms for PCH GPIO33 to EC GPIO13 connection and remove R159
- 8. Page 20, Change C634, C640 to 15pF
- 9. Page 23, Remove R108
- 10. Page 30, Change CON6 to vertical type for debug card
- 11. Page 33, Remove Q5, Q14 for Power switch LED and change R15 to 0 ohm
- 12. Page 34, Change J43 to eSATA connector and add C594~596, C698, C699 for eSATA solution, Remove C462
- 13. Page 34, Add U45, U46, C702, C704, R353, R362 for USB power protect switch and remove F4, F5
- 14. Page 38, Change PR183 to 4.7K to reduce the drop voltage
- 15. Page 39, Stuff ER46, EC102 for V_CHG
- 16. Page 40, Stuff PR161, PC137 for +3VSUS, PR174, PC149 for +5VSUS
- 17. Page 41, Stuff R247 1K ohms, No stuff R518, Change PR179 to 10.5K, R517 to 200K
- 18. Page 41, Stuff PR105, PC88 for +1_5VDIMM
- 19. Page 42, Stuff PR97, PC75 for +VTT
- 20. Page 43, Stuff PR35, PC26, PR34, PC21 for +VCC_CORE
- 21. Page 43, Change PC22 to 0.047uF, PR33 to 8.06K, PR115 to 2.32K, PR118 to 1.1K
- 22. Page 44, Stuff PR144, PC126 for +VCC_GFXCORE
- 23. Page 44, Change PC60 to 0.022uF, PC69 to 0.15uF, PR65 to 7.68K, PR73 to 18.2K, PR80 to 2.55K
- 24. Page 45, Change PR9 to 3.83K
- 25. Page 45, Stuff PR112, PC99 for VDDC and change PL5 to 1uH for reduce noise
- 26. Page 45, Change PR15 to 30K and stuff PC96 1uF for 1.8V_REG delay 1.2mS after +1_1V_1.0V_PWR
- 27. Page 45, Change PR11 to 1K and stuff PR145 100K to reduce current leakage
- 28. Page 46, Stuff PAD8 for EMI and add SCREW1, 2 in BOM. Remove BRAKET1
- 29. Page 49, Stuff CI54~64, CI70, CI85, CI87~90, CI92~97 for EMI
- 30. Page 16, Add PC158, PC161, Reserve C700, C701 for MVDDQ
- 31. Page 12, Add ATI debug point
- 32. Page 31, Add EMI cooper to seperate LAN GND
- 33. Page 32, Reserve R365 for cardreader issue
- 34. Page 45, Stuff PR18 13.3K, PQ5, PR23 10K for Park XT

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